Your Name (first last) _____ SID _____

UC Berkeley EECS151
Fall 2019 Midterm 2

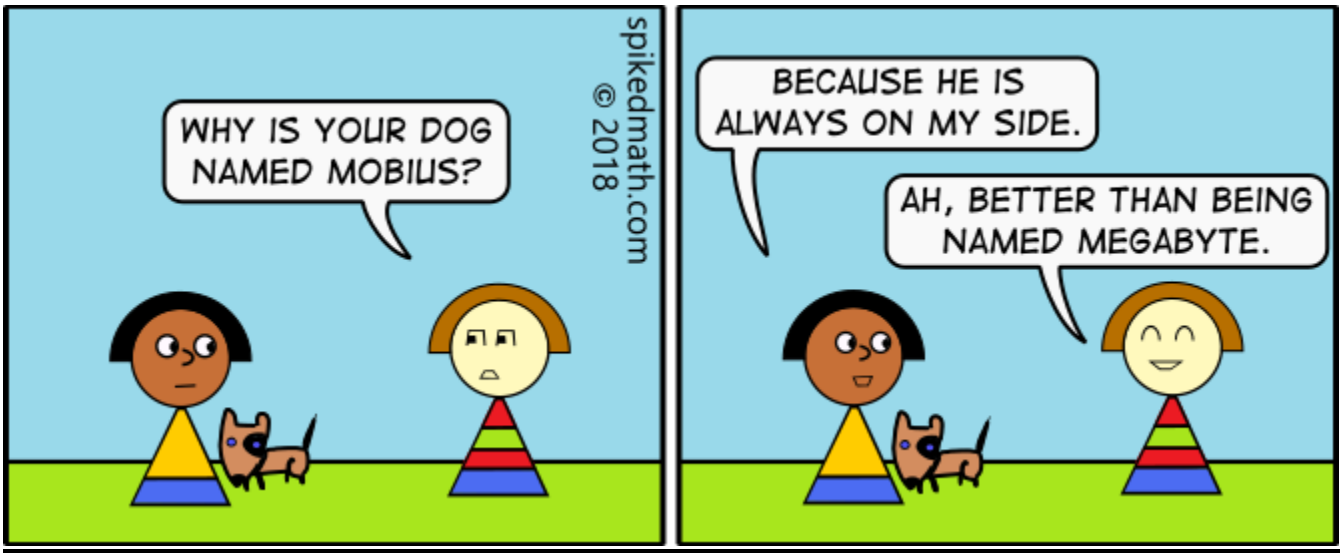
← Name of person on left (or aisle) _____

TA name _____

Name of person on right (or aisle) → _____

Fill in the correct circles & squares completely…like this: ● (select ONE), and ■ (select ALL that apply)

Question	1	2	3	4	Total
Minutes	20	26	12	22	**80**
Max Points	16	24	12	18	**70**
Points					



1) *It's all logical…* (16 points, 20 minutes)

a) The following function F that implements an OR-AND-Invert OAI21 gate.

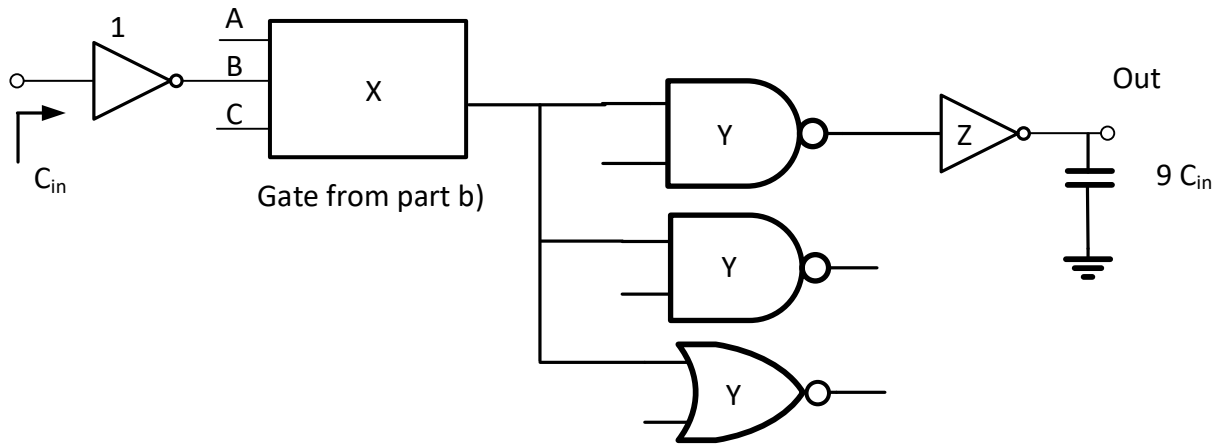
$$F = \overline{(A+B)C}$$

Implement the function F as standard, complementary CMOS logic gate. Size your transistors to match the pull-up/pull-down resistances to those of a unit inverter. You can assume NMOS and PMOS devices have equal strength in this technology.

b) Find the logical effort for the input B for the gate from part a).

g_B = _____.

c) The gate from part a) is used in the following circuit. Determine the gate sizes, X, Y, Z, that minimize the delay in the path below. If you're not confident about your answer to part c, assume the logical efforts of the new gate is 3. Gates sized as '1' have the equivalent driving resistance and input capacitance equal to a unit-sized inverter.



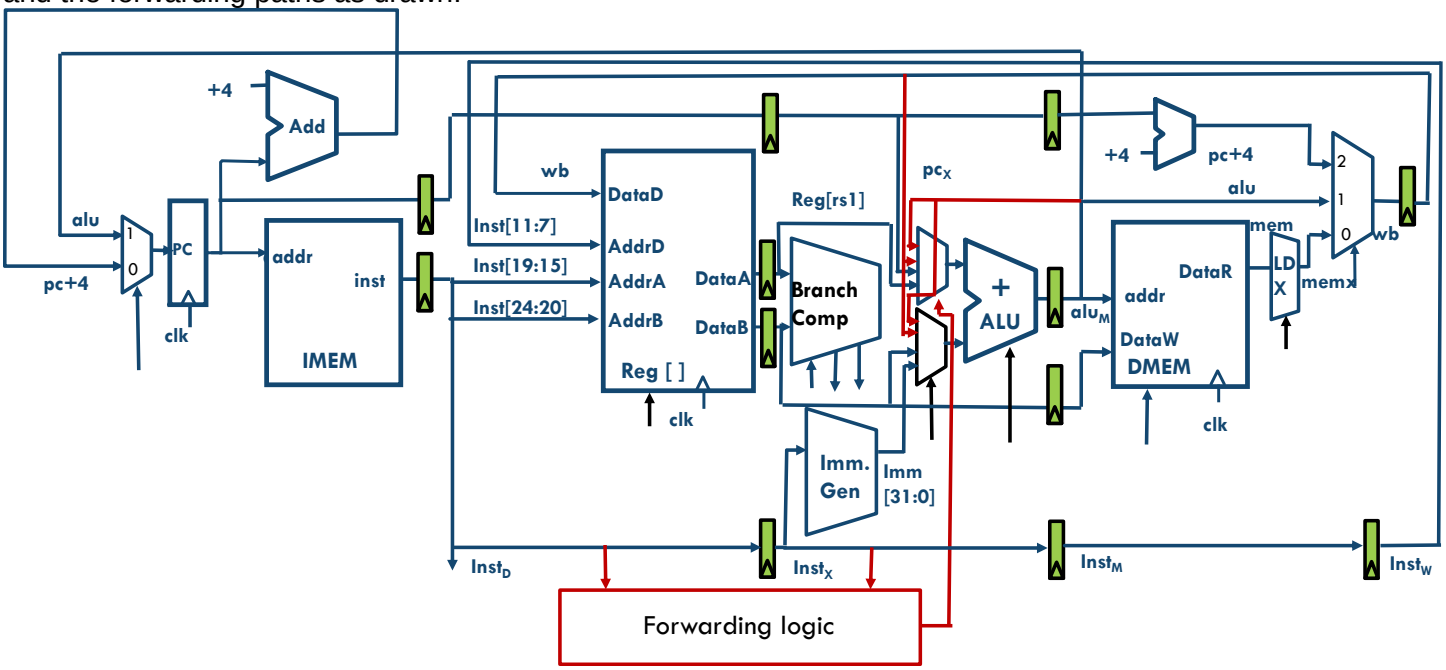
X = _____.

Y = _____.

Z = _____.

2) *RISC-V Pipelining and Hazards…* (24 points, 26 minutes)

Consider the 5-stage pipeline presented in lecture with combinational-read IMEM and DMEM and the forwarding paths as drawn.



Fill the pipeline diagrams for the following assembly program. Indicate when NOPs are injected into the pipeline by writing 'NOP'. Assume you can write to and read from the same address in the register file (Reg [ ]) in the same cycle. Consider two cases:

Case 1: The forwarding paths in the diagram are unused and all hazard resolution is accomplished with stalling.
Case 2: The forwarding mux in the diagram is driven correctly by the forwarding logic.

```
1            addi x1, x0, 0xFF
2            andi x2, x1, 0xF
3            bge x1, x2, label
4            xori x2, x2, 1
5            ori x3, x2, x1
6     label: lw x5, 0(x6)
7            sw x5, 4(x6)
```

Please write down instruction names in the pipeline diagram until the last instruction has written back to the regfile.

	Case 1					Case 2				
Cycle	F	D	X	M	WB	F	D	X	M	WB
1										
2										
3										
4										
5										
6										
7										
8										
9										
10										
11										
12										
13										
14										
15										
16										
17										
18										

b) Answer true or false for the following statements, about the 5-stage pipeline in this problem.

i) A mispredicted branch instruction causes 2 instructions to be killed

◯ True ◯ False

ii) Jumps (**`jal`**, **`jalr`**) cause 3 NOPs to be injected into the pipeline

◯ True ◯ False

iii) Using forwarding paths could increase CPI (clocks per instruction) over the stalling-only baseline

◯ True ◯ False

iv) Immediate generation, in general, can proceed in parallel with register file reads

◯ True ◯ False

v) Making the IMEM and the DMEM synchronous read would yield a 8-stage pipeline

◯ True ◯ False

vi) If the immediate generation was moved to the F stage, and you had an additional adder, you can make **`jal`** inject no NOPs

◯ True ◯ False

3) *Energy and Performance* (12 points, 12 minutes)

We would like to examine some properties of a single-cycle RISC-V datapath. The datapath presents a total load capacitance of 5pF to the supply, operates at 500 MHz, and has an activity factor of $\alpha_{\{0 \rightarrow 1\}}$=0.1. V_{DD} = 1V. The CPI is 1. You may find the following two equations useful for this problem.

$$\text{CPI} = \frac{\text{Clocks}}{\text{Instruction}}$$

$$\frac{\text{Seconds}}{\text{Program}} = \frac{\text{Instructions}}{\text{Program}} * \frac{\text{Cycles}}{\text{Instruction}} * \frac{\text{Seconds}}{\text{Cycle}}$$

a) What is the dynamic power consumption?

P = _____.

b) What is the average energy per instruction?

E_{inst} = _____.

c) How much energy is drawn from the supply to run a program with 1000 executed instructions?

E_{1000} = _____.

d) What is the energy-delay product for the case in c) ?

EDP = _____.

e) You are able to pipeline this design so a 5-stage pipeline operates at 1.5GHz, at the same supply V_{DD} = 1V, has the same activity factor, and has a CPI of 3. The load capacitance has increased by 50% compared to the non-pipelined baseline. Calculate the energy-delay product when running the same program as in c)

$EDP_{5\text{-stage}}$ = _____.

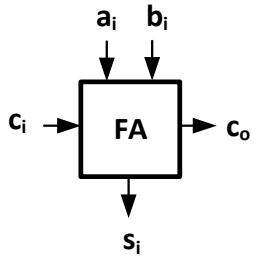
4) *Delays and Adders* (18 points, 22 minutes)

You are designing a datapath in a brand-new CMOS FinFET technology, where NMOS and PMOS devices have equal strength. In particular, it has only four CMOS gates: 2- input NAND, 2-input NOR, 2-input XOR, and an OAI21 gate ($Y = \overline{(A+B)C}$). Gate capacitance equals drain capacitance per unit area ($\gamma = 1$), and the four gates come in with only one size each, i.e., you do not need to size gates in this problem.

a) If both the 2-input NAND gate and the 2-input NOR gate have a delay dependence on a fanout, f, given as $t_{NAND2} = t_{NOR2} = 2ns(4 + 3f)$, what is the delay dependence on the fanout of the input C of the OAI21 gate (C is in the critical path)?

t_{AOI21} = _____.

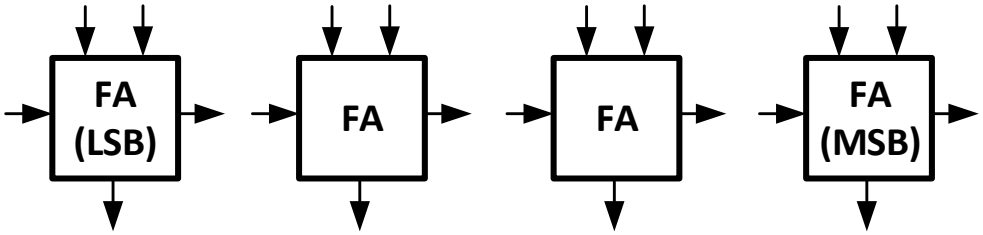
b) Draw a fast full-adder using the four types of gates and calculate the ci->sum and ci->cout delay. Note that using an OAI21 gate could potentially simplify the logic for C_out. Assume the capacitance driven by the sum and the carry bits is equal to the capacitance of inputs a_i, b_i and $t_{XOR2} = 2ns\ (8 + 8f)$.



$t_{FA,Ci\rightarrow Co}$ = _____.

$t_{FA,Ci\rightarrow S}$ = _____.

c) Complete the drawing and label all inputs and outputs for an 4-bit ripple-carry adder in figure below by using full-adder (FA) cells from part b). Inputs are a[3:0] and b[3:0] and there is no carry-in to the least-significant bit.



d) Find the critical path delay for the circuit in part c), if the capacitance driven by the sum and the carry bits is equal to the input a_i, b_i capacitance. If you are not confident in your answer in part b), you can express the delay in terms of $t_{FA,Ci\rightarrow Co}$, and $t_{FA,Ci\rightarrow S}$

Critical path = _____.