Problem 1

: (DC analysis, resistor combinations, Thevenin and Norton equivalent circuits): For each circuit, find the specified current, voltage and/or equivalent circuit. Hint: you may use source transformations where and if appropriate. (5 points each).

a. Find the current $i$ and the voltage $v$ (no mesh or nodal analysis).

b. Find $R_{eq}$. All resistances are in Ohms. (NO mesh or nodal analysis).

c. Find the voltage $v_1$. 
Problem 2

(Operational amplifiers, ideal op-amp techniques): Find \( v_0/v_s \) for the circuit shown below (13 points). Assume that the operational amplifiers are ideal and that an ideal amplifier has an

\[ A = \infty \] (infinite). State the properties of an ideal operational amplifier (2 points).

Problem 3

(Capacitor voltage initial condition, forced and transient response): For the circuit shown below, find \( i(t) \) for \( t>0 \). Assume the circuit is in steady state at \( t=0 \). Hint: Voltages across capacitors cannot change instantaneously. \( 0+ \) denotes time and \( t=0+ \). The current source \( 10u(t) \) mA signifies that its value (i.e. the value of the source current) is equal to 0 A (or alternatively the source is "dead") for time \( t<=0 \), and equal to a 10 mA source for \( t>0 \). (15 points)
Problem 4

(Sinusoidal steady-state analysis including phasors and impedances. Frequency response and Bode asymptotic plots):

a. A circuit is shown below with a voltage source equal to \( v_s = 100 \cos 1000t \) V. (8 points – no partial credit)

For the circuit shown find:

(a1) the impedance \( Z \)

(a2) using \( Z \), find the phasor current \( I \)

(a3) find \( i(t) \)

b. An operational amplifier circuit is shown below. Find the ratio \( V_o / V_s \) as a function of \( \omega \) (4 points) and sketch the asymptotic Bode plot when \( R_2 = 10 R_1 \) and \( R_2 C = 0.1 \) . (It should show the corner frequency \( \omega_c \) and the frequency \( \omega_m \) where it crosses the \( \omega \) axis). (4 points)

Problem 5
a. Fill the following truth table (5 points)

b. Use the Karnaugh map to find the minimum function F.

c. Implement using only two-input NAND gates (i.e. the gate has only two inputs). You can assume that the input complements are available. (5 points)

Problem 6

: (Sequential logic with D flip-flops, state table, state diagram, timing diagram): A sequential circuit with two D-type flip-flops A and B (i.e. with inputs D_A, D_B and respective outputs A and B), two input variables X and Y, and one output variable Z is specified by the following input equations:
\[ A = (\overline{X})Y + XA \ , \ D_B = (\overline{X})B + XA \ , \ \text{and} \ Z = B. \]

a. Draw the logic diagram of the circuit (6 points)

b. Fill up the state table (7 points). Hint: Take all possible combinations of inputs and initial states.

c. (you can either do c_1 or c_2) [c_1] draw the state diagram or [c_2] fill in the timing diagram. (7 points)

\[ c_1 \]

\[ c_2 \]
Solutions:

1a) $i = 3.33$ A, $v = -13.33$ V

b) $R_{eq} = 14$ Ohms

c) $v_1 = 10$ V

d) $V_T = 16$ V, $R_T = 16/3$ Ohms

2) $(V_o/V_s) = 22$

3) $i(t) = -2 + (10/3)e^{-2000t}$ mA

4a) $Z = 2 + j = 5^{1/2} \angle 6.7^\circ$ Ohms

a2) $447 \angle -26.7^\circ$ A

a3) $i(t) = 44.7\omega (1000t - 26.7^\circ)$ A

b) $(V_o/V_s) = 1/(1 + j\omega R_2 C)$

5a)

Truth table:
b) K map for F:
\[ \begin{array}{c|c|c|c|c}
A & B & C & F \\
0 & 0 & 0 & 1 \\
0 & 0 & 1 & 1 \\
0 & 1 & 0 & 1 \\
0 & 1 & 1 & 0 \\
1 & 0 & 0 & 1 \\
1 & 0 & 1 & 0 \\
1 & 1 & 0 & 0 \\
1 & 1 & 1 & 0 \\
\end{array} \]

```c\AB 00 01 11 10
0
11 0 1
1
1 0 0 0
```

c) A----\D----\ 
| | D ----------- D \ 
B--D----/ / 
| | | D - F 
C----| / 
| / 
D -----------/