UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

Professor Oldham

Fall 2000

EECS 40 — FINAL EXAM

Saturday, 16 December 2000, 8:00 - 11:00 a.m.

Name: _____ **Student ID:** _____
Last, First

Signature: SOLUTIONS

TA: ❑ Ben
❑ Warren
❑ Naratip

Guidelines:

1. Closed book and notes except 1 page of formulas.
2. You may use a calculator.
3. Do not unstaple the exam.
4. Show ***all your work and reasoning on the exam*** in order to receive full or partial credit.
5. **Caution**: NO CREDIT will be given for answers not in answer boxes.
6. This exam contains 8 problems and corresponding worksheets plus the cover page.

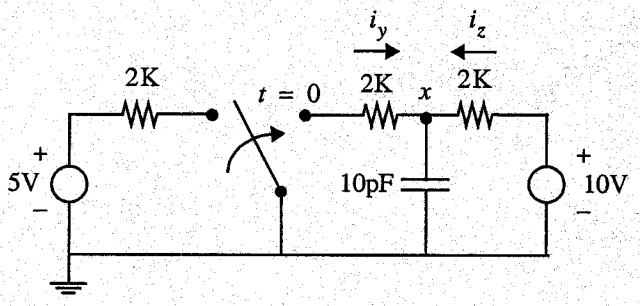
Problem	Points Possible	Your Score
1	12	
2	12	
3	12	
4	12	
5	14	
6	12	
7	12	
8	14	
Total	**100**	

$\varepsilon_o = 8.85 \times 10^{-14}$ F/cm

$f = 10^{-15}$
$p = 10^{-12}$
$n = 10^{-9}$
$\mu = 10^{-6}$
$m = 10^{-3}$
$K = 10^{3}$
$M = 10^{6}$

Problem 1 (12 points)

(a)



The switch closes at $t = 0$.

(a.1) What is V_x at $t = 0^+$?

a.1 $V_x(t = 0^+) = 10\,V$

(a.2) What is i_y at $t = 0^+$?

$$i_y(t=0^+) = \frac{0 - V_x(t=0^+)}{2k}$$

$$= \frac{-10}{2k} = -5\,mA$$

a.2 $i_y(t = 0^+) = -5\,mA$

(a.3) What is i_z at $t = 0^+$?

$$i_z(t=0^+) = \frac{10 - V_x(t=0^+)}{2k} = \frac{10-10}{2k}$$

$$= 0$$

a.3 $i_z(t = 0^+) = 0\,mA$

(a.4) What is $\frac{dV_x}{dt}$ at $t = 0^+$?

$$C\frac{dV_x}{dt} = i_y + i_z \Rightarrow \left.\frac{dV_x}{dt}\right|_{t=0^+} = \frac{-5+0}{C} = \frac{-5\,mA}{10\times10^{-12}\,F}$$

a.4 $\left.\frac{dV_x}{dt}\right|_{t=0^+} = -5\times10^{8}\left(\frac{V}{sec}\right)$

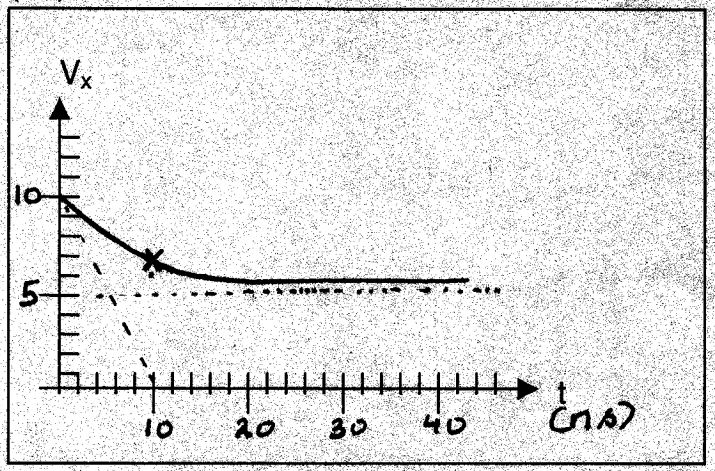
(a.5) Draw very neatly the graph of V_x versus time on the axes provided opposite. (You MUST put scales on the axes to receive full credit.)

(a.6) Write an equation for $V_x(t)$.

a.6 $V_x(t) = 5 + 5\exp(-t/10^{-8})$

Problem 1 (Cont.)

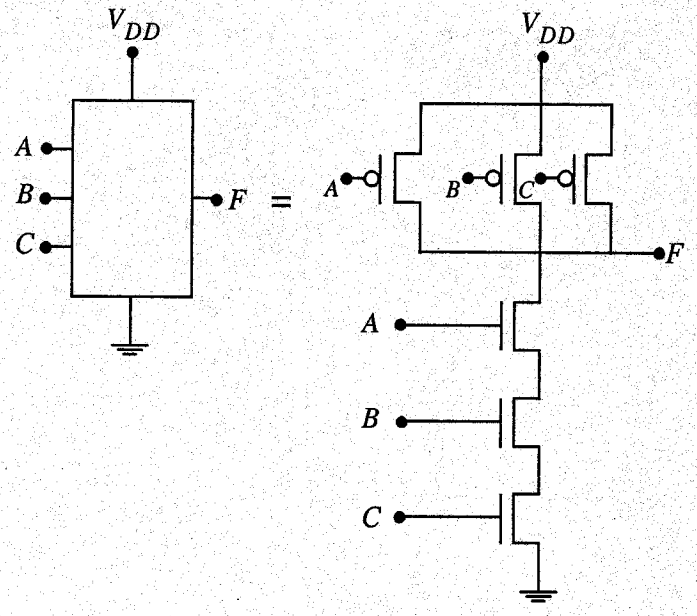
(a.5)



The * shows the value of V_x at t = time constant = 10 ns

Problem 2 (12 points)

(a)



PMOS Device Parameters

$|V_T| = 0.5\text{V}$

$\left.\frac{W}{L}\right|_p = \frac{0.75}{0.25}$

$R_P = 3\text{K}$ $\quad C_{Dp} = 1f\text{F}$

$C_{Gp} = 6f\text{F}$

NMOS Device Parameters

$|V_T| = 0.5\text{V}$

$\left.\frac{W}{L}\right|_n = \frac{0.75}{0.25}$

$R_N = 1.5\text{K}$ $\quad C_{Dn} = 1f\text{F}$

$C_{Gn} = 6f\text{F}$

(a.1) Fill out the Truth Table. (Define logic "1" as $\sim V_{DD}$ and logic "0" as $\sim 0V$.)

a.1

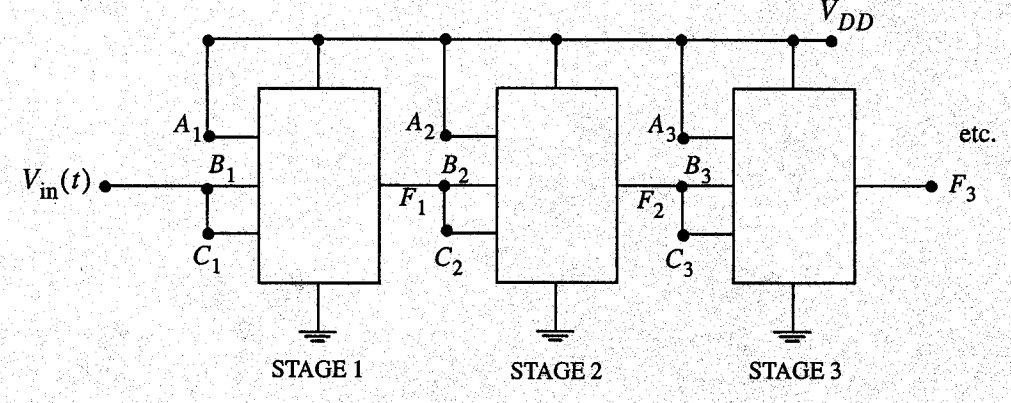
A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(a.2) What is the logic function (F in terms of A, B, C)?

a.2

$F =$ $\overline{A \cdot B \cdot C}$

(b) A number of these gates are hooked up as follows:



Problem 2 (Cont.)

(b.1) If $V_{in}(t)$ is initially zero and suddenly jumps to V_{DD}, can you write an expression for the stage delay τ_{DHL}, i.e., the time it takes F_1 to go from V_{DD} to $V_{DD}/2$ (in terms of device parameters R_n, R_p, C_{Dn}, C_{Dp}, C_{Gn}, C_{Gp})? **Note**: Ignore wiring capacitance and do not evaluate numerically.

b.1

$\tau_{DHL} = 0.69 \cdot R \cdot C$ where

$R = 3Rn$ and

$C = 3C_{DP} + C_{DN} + 2C_{GP} + 2C_{GN}$

(formulas only)

(b.2) In the same circuit above $V_{in}(t)$ is a square wave going from 0 to V_{DD} to 0, etc. We are interested in worst case delay. Which transient is slower: τ_{DHL} or τ_{DLH}? Answer the question by checking one of the three boxes.

b.2

- ☐ $\tau_{DLH} > \tau_{DHL}$
- ☒ $\tau_{DLH} < \tau_{DHL}$
- ☐ $\tau_{DLH} = \tau_{DHL}$

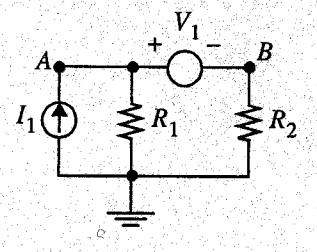
(b.3) Why? (Explain answer to **b.2**.)

b.3

$3Rn > Rp$

Problem 3 – Circuit Analysis (12 points)

(3 marks)
(a)



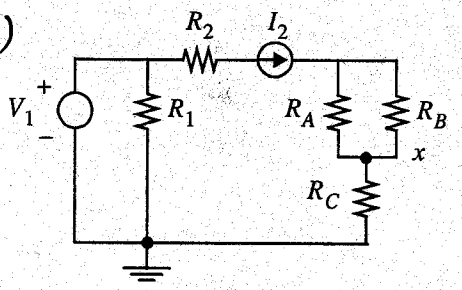
Find V_B in terms of V_1, I_1, R_1, R_2.

$I_1 = \frac{V_A}{R_1} + \frac{V_B}{R_2}$

$V_A = V_1 + V_B$

$V_B = \frac{(I_1 R_1 - V_1) R_2}{R_1 + R_2}$

(3 marks)
(b)

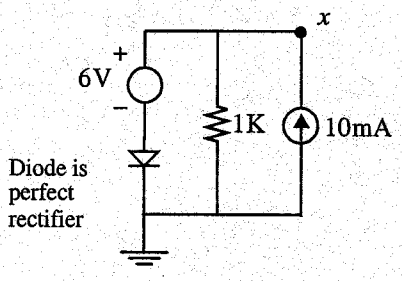


Check "Yes" or "No" for each item in the following table:

		Yes	No
V_x depends on	V_1 ?		×
"	R_1 ?		×
"	R_2 ?		×
"	R_A ?		×
"	R_B ?		×
"	R_C ?	✓	

$V_x = I_2 R_C$

(2 marks)
(c)

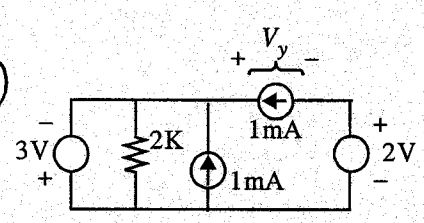


Find V_x.

Since diode is a perfect rectifier, no voltage drop can exist across it.

$V_x = 6\,V$ (V)

(2 marks)
(d)

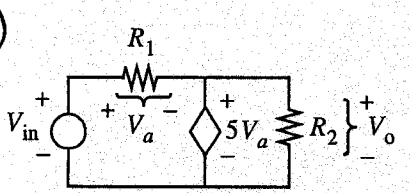


Find V_y.

Apply KVL on the outermost loop.

$V_y = -5\,V$ (V)

(2 marks)
(e)



Find V_o in terms of V_{in}, R_1, R_2.

$V_{in} = V_a + 5V_a = 6V_a$

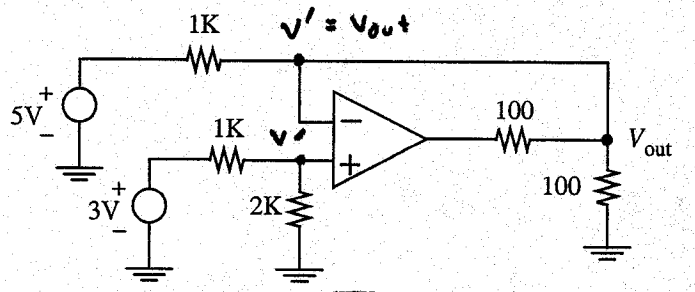
$V_o = 5V_a$

$V_o = \frac{5}{6} V_{in}$

Problem 4 – Op-Amp Circuits (12 points)

Note: Assume that all op-amps are ideal except that they have rails of ±5V.

(a)



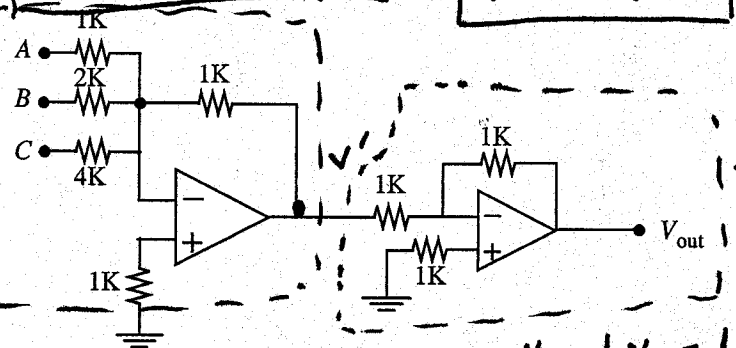
Find V_{out}.

$V' = \frac{(3V)(2K)}{1K+2K} = 2V$ (Voltage divider)

$V' = V_{out} = 2V$

$V_{out} = 2$ (V)

(b)



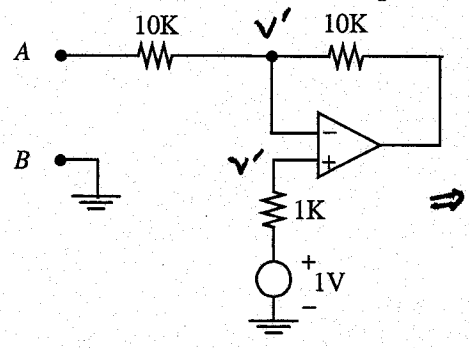
Fill out the table:

V_A	V_B	V_C (V)	V_{out} (V)
0	0	0	0
0	0	2	0.5
0	2	0	1.0
0	2	2	1.5
2	0	0	2.0
2	0	2	2.5
2	2	0	3.0
2	2	2	3.5

$V' = -\left(\frac{V_A}{1K} + \frac{V_B}{2K} + \frac{V_C}{4K}\right)(1K) = -V_A - \frac{1}{2}V_B - \frac{1}{4}V_C$

$V_{out} = -V' = V_A + \frac{1}{2}V_B + \frac{1}{4}V_C$

(c) Find and sketch the Thévénin Equivalent of this op-amp circuit (from terminals A-B).

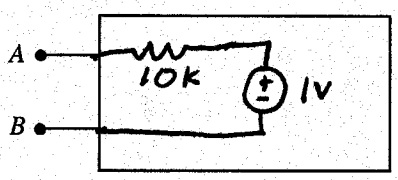


$V_{OC} = V' = 1V$

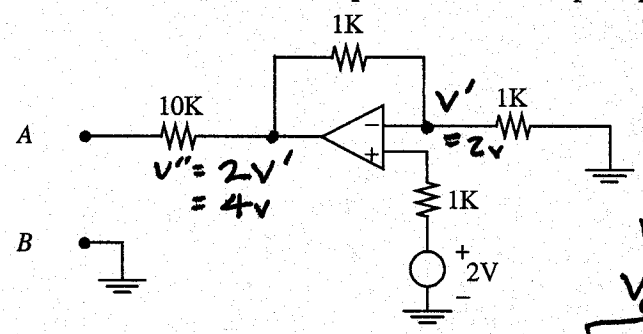
$I_{SC} = \frac{V'}{10K} = \frac{1V}{10K}$

$\Rightarrow R_T = \frac{V_{OC}}{I_{SC}} = \frac{1V}{1/10K}$

$R_T = 10K$



(d) Find and sketch the Norton Equivalent of this op-amp circuit (from terminals A-B).

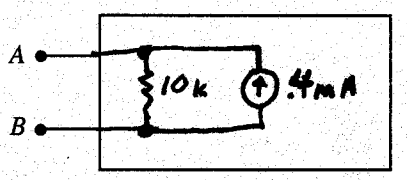


$V'' = 2V'$

$V_{OC} = 4V$

$I_{SC} = 4V/10K = .4mA$

$R_T = \frac{V_{OC}}{I_{SC}} = 10K$



Problem 5 (14 points)

A CMOS process is listed below:

(1) Start with p-type wafer.
(2) Deposit 0.5μm oxide. Note: This and all oxides have relative dielectric constant of 3.9. (ε_0 is on cover page.)
(3) Pattern with well mask. (LIGHT GRAY, DARK FIELD)
(4) Implant n well and drive to 1μm depth.
(5) Remove all oxide and deposit 0.5μm oxide.
(6) Pattern with active area mask. (BLACK RECTANGLE, DARK FIELD)
(7) Grow 10nm gate oxide.
(8) Deposit 0.5μm polysilicon.
(9) Pattern polysilicon (gates). (DARKER GRAY, CLEAR FIELD)
(10) Apply resist and pattern with select mask. (NOT SHOWN)
(11) Implant p-type source drains and anneal to get 0.1μm junction depth.
(12) Apply resist and pattern with second select mask. (NOT SHOWN)
(13) Implant n-type source drains and anneal to get 0.5μm junction depths for both p-type and n-type source drains.
(14) Deposit 0.5μm oxide.
(15) Pattern for contacts. (LIGHTER SQUARES IN ACTIVE AREA, DARK FIELD)
(16) Deposit 1μm Al metal.
(17) Pattern metal. (DOTS, CLEAR FIELD)

We do not show the layout for the entire circuit, but just one PMOS device on page opposite.

(a) Draw a sketch on the axes provided (on the facing page) of the cross-section through the device along the line A-A (after step 17). **Note**: The sketch must be to scale and neat to receive full credit.

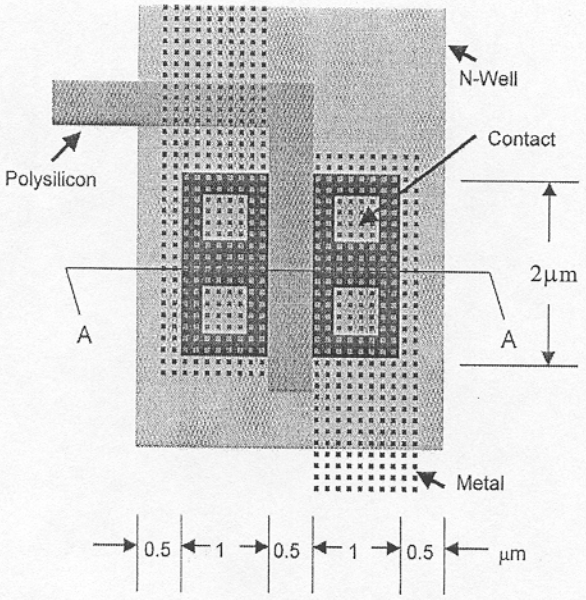
(b) What is the gate capacitance in *f*F of this device? (Put answer in box provided on facing page.)

$C_G = \frac{\varepsilon_r \varepsilon_0}{t_{ox}} \cdot W \cdot L = \frac{3.9 \times 8.85 \times 10^{-14}}{10^{-6}} \cdot .5 \times 10^{-4} \cdot 2 \times 10^{-4} = 3.4 \times 10^{-15}\ F$

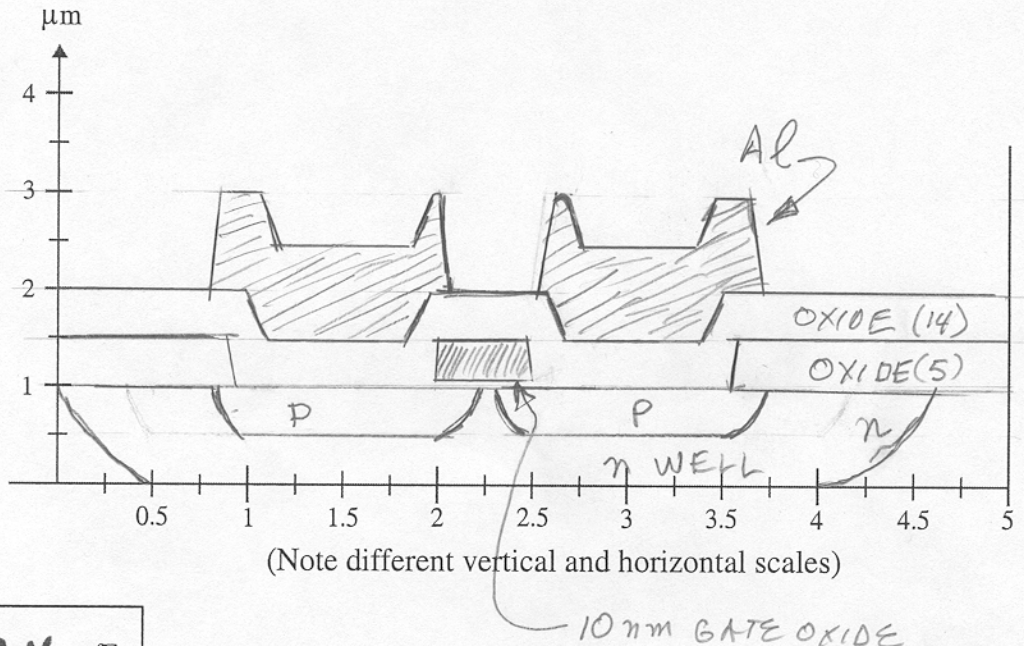
(c) What is the metal to substrate capacitance per unit area (*f*F/(μm)^2 ? (Put answer in box provided on facing page.)

$C_{MA} = \frac{\varepsilon_r \varepsilon_0}{t_{field}} = \frac{3.9 \times 8.85 \times 10^{-14}}{1 \times 10^{-4}} = \frac{0.034 \times 10^{-15}\ F/cm^2}{10^{-8}}$

Problem 5 Answer Sheet



(a)



(Note different vertical and horizontal scales)

10 nm GATE OXIDE

(b) C_{Gp} = **3.4** *f*F

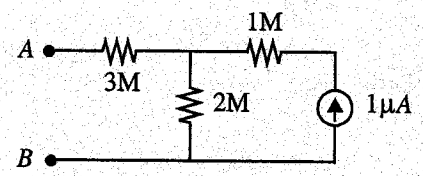
NOTE – 0.5μm JUNCTION DEPTH IS TOO DEEP! THEY WILL SHORT UNDER GATE

(c) C_{MA} = **0.034** *f*F/μm²

Problem 6 (12 points)

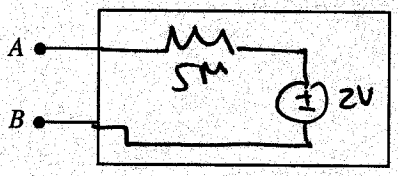
Find the Thévénin equivalent circuits of the following. (You **must** draw solution in box provided.)

a)

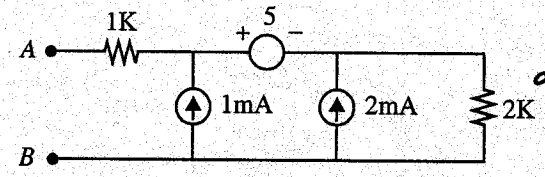


$R_{TH} = 3M + 2M = 5M$

$V_{TH} = (2M)(1\mu A) = 2V$



b)



(Hint: Use Superposition)

$R_{TH} = 1k + 2k = 3k$

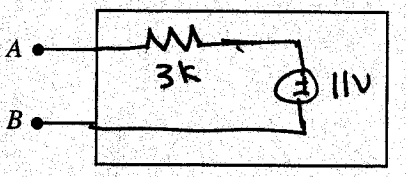
V_{TH} by Superposition due to

$1mA \rightarrow 2V$

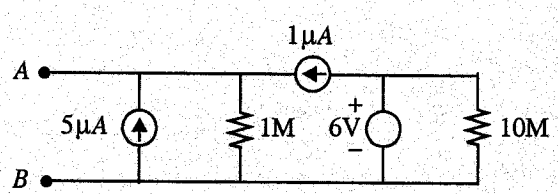
$2mA \rightarrow 4V$

$5V \rightarrow 5V$

$V_{TH} = 11V$

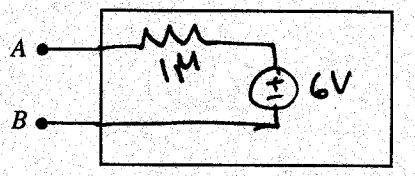


c)

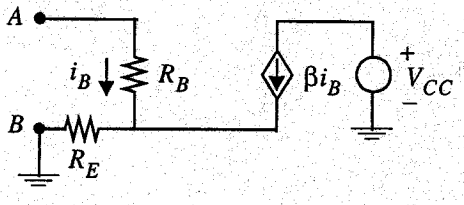


$R_{TH} = 1M$

$V_{TH} = (5+1)(1) = 6$



d)



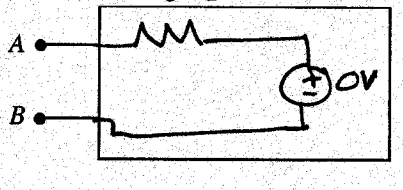
V_{TH} / $i_b = 0 \Rightarrow V_{AB} = 0$

R_{TH} / Use 1V test

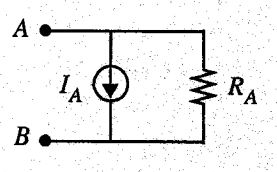
$R_{TH} = 1/I_B$

$I_B = \dfrac{1 - (\beta+1) I_B R_E}{R_B}$

$I_B \left[1 + (\beta+1)\dfrac{R_E}{R_B}\right] = \dfrac{1}{R_B} \Rightarrow \dfrac{1}{I_B} = R_{TH} = R_B + (\beta+1)R_E$

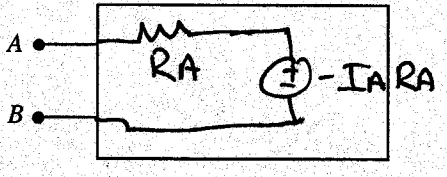


e)



$R_{TH} = R_A$

$V_{TH} = -I_A R_A$



Problem 7 – Power and Energy (12 points)

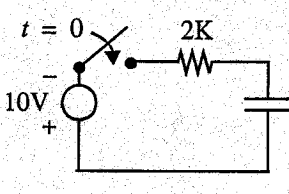
(a) The switch closes at $t = 0$. Then we wait a long time. Find the energy:

(a.1) delivered by the power supply.

(a.2) dissipated in the resistor.

(a.3) delivered to the capacitor.

(Answers **must** appear in answer boxes and **must** have units.)



(initially uncharged)

$CV^2 = 0.1\text{mJ}$

a.1 0.1 units mJ

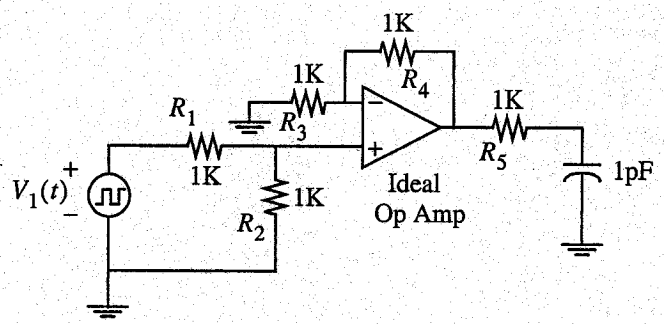
$\frac{1}{2}CV^2 = 0.05\text{mJ}$

a.2 0.05 units mJ

$\frac{1}{2}CV^2 = 0.05\text{mJ}$

a.3 0.05 units mJ

(b)



$V_1(t)$ is a square wave switching every 1μsec. It is going from +2V to 0V, back to +2V, etc. (Period is 2μsec.)

(b.1) What is the average power delivered by V_1 in mW?

$P_{av} = \frac{1}{2}\frac{V^2}{(R_1+R_2)} = \frac{1}{2}\frac{(2)^2}{2k} = 1\text{mW}$

b.1 $P =$ 1 mW

(b.2) What is the average power dissipated in each of the resistors R_1 to R_5?

R_1, R_2, R_3, R_4 have same voltage drops.

$P_{R1-R4} = \frac{1}{2}\frac{V^2}{R} = \frac{1}{2}\frac{(1)^2}{1k} = 0.5\text{mW}$

op amp output voltage is a square wave 0 to 2V

$P_{R5} = \frac{1}{2}CV^2f = \frac{1}{2}(1p)(2)^2(10^6)$

b.2

$P_{R1} =$ 0.5 mW

$P_{R2} =$ 0.5 mW

$P_{R3} =$ 0.5 mW

$P_{R4} =$ 0.5 mW

$P_{R5} =$ 0.002 mW

(b.3) What is the average power dissipated in the capacitor? = 2μW

Capacitor does not dissipate any (average) power.

b.3 $P =$ 0 mW

(b.4) Where does the energy dissipated in R_3 come from?

b.4 op amp power supply ?

Problem 8 – Drain I-V (14 points)

The drain I-V characteristics of one of the Berkeley world record-setting PMOS "FinFet" devices are given opposite. The device has a channel length of only 40 nm. This device has a width of 1μm and a gate oxide thickness of 2 nm. If we assume a (−)0.25V threshold, we note that in saturation it seems to obey our model equation:

$$I_D = I_{DS}(1 + \lambda|V_{DS}|)$$

where

$$I_{DS} = k_V \frac{W}{L}(V_{GS} - V_T).$$ (Note: V_{GS}, V_{DS}, I_D, I_{DS}, V_T are all negative for PMOS.)

We intend to use this device in a circuit with logic values corresponding to ~0V and ~1V, using, of course, a 1V power supply.

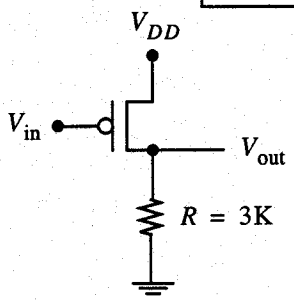
(a) Device parameters: **a.1)** What is k_V for this device (20% accuracy)?

k_V = 16 units μA/V

a.2) What is λ (20% accuracy)?

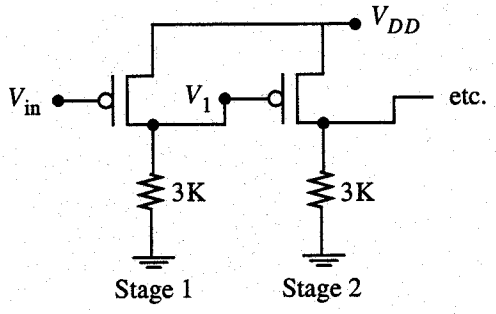
λ = 0.1 units V^{-1}

(b) Basic inverter: In the absence of an NMOS device we can still make an inverter with a resistor and power supply. Suppose we hook up the device as follows:



(b.1) For this inverter you are to estimate the output voltage at several values of input voltage; in particular, fill out the table opposite. An accuracy of .05 V is adequate.

In order to estimate the performance of this CMOS inverter, we consider a chain of identical inverters. Stage 1 and 2 are shown at the right. Suppose the input to stage 1 is low (~0V).



(b.2) The Berkeley designers believe that for this inverter a sensible logic "0" range might be $0 < V < 0.25$V. What might be a sensible voltage range to define as "1"?

b.2 0.75 < V < 1

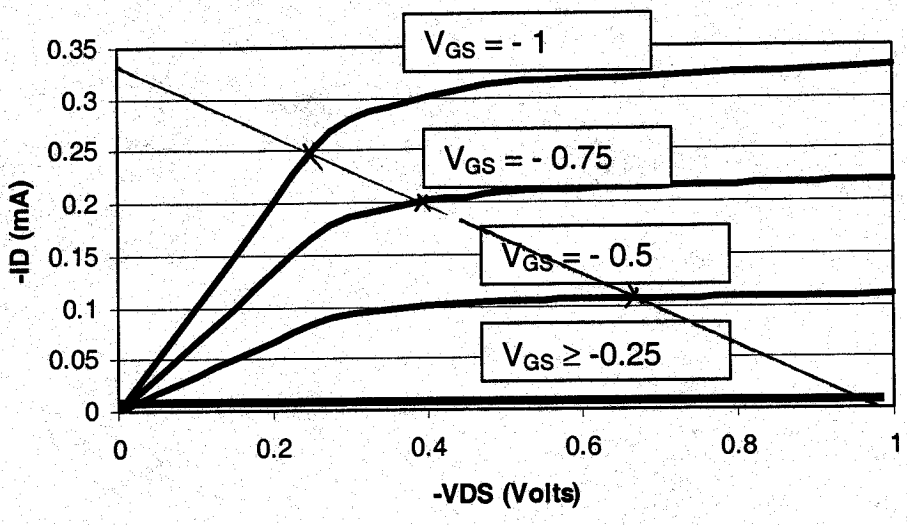
(b.3) Now we want to consider the transient. If we ignore interconnect and drain capacitances, what is the capacitance loading the output node of stage 1? Give both a formula in terms of the circuit capacitances and evaluate for the numerical value.

b.3 $C = \frac{\varepsilon_{ox}}{t} \cdot W \cdot L$ (formula)

C = 0.69 (fF) (numerical value)

(b.4) The input to stage 1 is suddenly switched from 0V to 1V. We expect the output of stage 1 to go from high to low. You have already computed the capacitance in question (b.3); now compute the resistance governing this transient. And compute the time for the output to reach 0.25V (formula and value). PLEASE NOTE ANSWER BOXES OPPOSITE.

Problem 8 (Cont.)



(b.1)

V_{in}	V_{GS}	V_{out}
0	1	0.75
0.25	0.75	0.6
0.5	0.5	0.35
0.75	0.25	0
1.0	0	0

(b.4) R = 3K ohms

$\Delta t = -RC \ln \frac{V_{OL}}{V_{OH}}$ (formula)

Δt = 2.8×10^{-12} (sec)