EECS 40 — MIDTERM #2
10 November 1999

Guidelines:

1. Closed book and notes except 1 page of formulas.
2. You may use a calculator.
3. Do not unstaple the exam.
4. Show all your work and reasoning on the exam in order to receive full or partial credit.
5. This exam contains 12 pages plus the cover page and 2 sheets of scratch paper included at the end of the exam. You can remove these from the rest of the exam if you wish.

<table>
<thead>
<tr>
<th>Problem</th>
<th>Points Possible</th>
<th>Your Score</th>
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<td>1</td>
<td>20</td>
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<td>Total</td>
<td>100</td>
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K = 10^3
m = 10^{-3}
μ = 10^{-6}
n = 10^{-9}
p = 10^{-12}
f = 10^{-15}
Problem 1 (20 points)

What is the value of the unknown node voltage in each of the following circuits? Assume diodes are perfect rectifiers.

(a)  

![Diagram](5V to 6V, 10V to 9V, 100K resistor)

\[ V_X = \_ \_ \_ \_ \_ \_ \_ \_ \_ \]

(b)  

![Diagram](12V, 100K resistor)

\[ V_Y = \_ \_ \_ \_ \_ \_ \_ \_ \_ \]

(c)  

![Diagram](25V, 100K resistor)

\[ V_Z = \_ \_ \_ \_ \_ \_ \_ \_ \_ \]

(d)  

![Diagram](77V)

\[ V_{AB} = \_ \_ \_ \_ \_ \_ \_ \_ \_ \]

(e)  

![Diagram](77V)

\[ V_{CD} = \_ \_ \_ \_ \_ \_ \_ \_ \_ \]

(f) A cross-section for a CMOS chip is shown on the facing page. Some node voltages are indicated. Please tell us what the values are for the node voltages at nodes U, W, R, S.

\[ V_U = \_ \_ \_ \_ \_ \_ \_ \_ \_ \]

\[ V_W = \_ \_ \_ \_ \_ \_ \_ \_ \_ \]

\[ V_R = \_ \_ \_ \_ \_ \_ \_ \_ \_ \]

\[ V_S = \_ \_ \_ \_ \_ \_ \_ \_ \_ \]
Problem 2 (20 points)

Shown on the opposite page is the layout and two cross-sections through a CMOS inverter. A list of components follows. You are to indicate, by labelling, the location of that feature on the figure. The first question is used as an example.

2.1 Layout

(1) A contact to polysilicon [EXAMPLE]
(2) gate of NMOS transistor
(3) the W dimension of the PMOS transistor
(4) contact to p-type substrate
(5) metal contact to PMOS gate
(6) spacing from n+ source gain areas to well mask
(7) input electrode
(8) output electrode

2.3 Masks

A possible list of masks for this process follows. You are to order the masks by simply filling in the mask number. It is possible that one or more masks is missing. If so, you must fill out a new mask row for each missing mask.

<table>
<thead>
<tr>
<th>MASK#</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly</td>
<td>Define polysilicon areas</td>
<td></td>
</tr>
<tr>
<td>N-select</td>
<td>Define n+ implant areas</td>
<td></td>
</tr>
<tr>
<td>P-select</td>
<td>Define p+ implant areas</td>
<td></td>
</tr>
<tr>
<td>Oxide</td>
<td>Define areas for gate oxide</td>
<td></td>
</tr>
<tr>
<td>Metal</td>
<td>Define metal conductor pattern</td>
<td></td>
</tr>
</tbody>
</table>

Fill in mask # here

2.4 Gate delay

For this layout, what do we expect for the relationship between gate delay for output rising (t_{pLH}), and output falling (t_{pHL})? Answer by putting in the correct symbol in the box (=, >, or <).

Put symbol here  

\[ t_{pLH} \quad \quad t_{pHL} \]

Why? ____________________________________________________________
Prob. 2 – Schematic for CMOS Inverter
Problem 3 (20 points)

You are trying to construct a dc switch with an MOS transistor, as shown below. The idea: When input is low, output high. But when input is high, output is hopefully low.

![Diagram of MOS transistor circuit]

(a) If $V_{IN} = 5\, \text{V}$, what is the channel electron charge (coulomb/cm$^2$) (for small values of $V_{OUT}$ only)?

   formula: __________________

   value: _________________

(b) If $V_{IN} = 5\, \text{V}$, what is the sheet resistance of the channel? (Again for the case in which $V_{OUT}$ is very small.)

   formula: __________________

   value: _________________

(c) What is the value of $V_{IN}$ needed to produce an output of 0.1 V?

   $V_{IN} =$ __________________

(d) If the input suddenly switches low, and the load is 10 pF, as shown, sketch the output voltage versus time (accurately) and estimate the time $\Delta t$ for the output to go from 0.1 V to 2.45V (halfway to 5 V).

   $\Delta t =$ __________________n sec
Problem 3 Answer Sheet

(d)

\[ V_{OUT}(V) \]

\[ \text{time} \]
Problem 4 (20 points)

A CMOS inverter drives an off-chip capacitance load, as shown below. All you know about the MOS transistors is shown in the graphs. (DO NOT ASK for more information!)

(a) Draw the circuit model (in the box provided on opposite page) for the circuit (replacing transistors with appropriate simpler elements, such as voltage sources, current sources, resistors, capacitors, inductors) when \( V_{\text{IN}} = 3 \) V. No numerical values are required in part (a).

(b) Suppose \( V_{\text{IN}} \) suddenly switches to 0V at \( t = 0^+ \). Draw the new circuit model in the box provided (again with simpler elements). Show both the general form and the numerical values for all parameters.

(c) Sketch the form of \( V_{\text{OUT}} \) versus time for \( t = 0^+ \) to \( t \to \infty \) on the axes provided. (No numbers needed.)

(d) What is the time delay for \( V_{\text{OUT}} \) to go to \( V_{\text{DD}}/2 \) (in n sec)?

\[ \Delta t = \underline{\phantom{00000}} \text{nsec} \]

(e) At what time does \( V_{\text{OUT}} \) equal 1 V (in n sec)?

\[ t = \underline{\phantom{00000}} \text{nsec} \]
Prob. 4 Answer Sheet (Parts a, b, c)

(a) PUT CIRCUIT HERE for $V_{IN} = 3V$

(b) PUT CIRCUIT HERE for $V_{IN} = 0$

(c) $V_{OUT}(t)$ vs. $t$ graph
Problem 5 (20 points)

(a) You open up your Robot Kit and find the following circuit. You suspect it is a linear voltage amplifier. You know the differential amplifier has very high internal gain.

(a.1) Is it a linear amplifier?

(a.2) If so, what is the voltage gain $\frac{V_o}{V_i}$? [If not, ignore (a.2).]

(a.3) If not, why not?

(b) You also find the following circuit. Again you suspect a linear amplifier. You know the differential amplifier has very high internal gain.

(b.1) Is it a linear amplifier?

(b.2) If so, what is the voltage gain? [If not, ignore (b.2).]

(b.3) If not, why not?

(c) Carefully sketch the curve of $V_{OUT}$ versus $V_{IN}$ for circuit (a) on the graph axes provided for $0 \leq V_i \leq 250\text{mV}$.

(d) Carefully sketch the curve of $V_{OUT}$ versus $V_{IN}$ for circuit (b) on the graph axes provided for $0 \leq V_i \leq 250\text{mV}$.
Prob. 5. Answer Sheet

(c)

(d)