UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS 40
Introduction to Microelectronic Circuits

Fall 2003
Prof. King

MIDTERM EXAMINATION #2
November 3, 2003
Time allotted: 50 minutes

NAME: SOLUTIONS, _______________________
(print) Last First

Signature: ___________________________ STUDENT ID#: ___________________________

Discussion Section: __________

1. This is a CLOSED BOOK exam. However, you may use 2 sheets of notes and a calculator.

2. SHOW YOUR WORK or REASONING on this exam.
   (Make your methods clear to the grader.)

3. Write your answers clearly (legibly) in the spaces (lines, boxes, or plots) provided.

4. Remember to specify the units on answers whenever appropriate.

SCORE: 1 _________ / 16

2 _________ / 17

3 _________ / 17

Total: _________ / 50
Problem 1: Energy-Storage Elements and 1st-Order Circuits [16 points in total]
a) Consider the capacitive voltage-divider circuit below. Find $V_{out}$. How will $V_{out}$ change if a small load capacitance $C_{load} < 2 \, \mu F$ is connected between terminals $a$ and $b$? [4 pts]

$$V_{out} = \frac{8 \, \mu F}{8 \, \mu F + 2 \, \mu F} (10 \, V) = 8 \, V$$

$V_{out}$ will [increase, decrease, not change] (circle one) when $C_{load}$ is connected, because the capacitance between terminals $a$ and $b$ will increase.

b) Consider the following RC circuit:

Provide a physical reason why it takes longer for $v_c$ to reach its final value if $R$ is increased. (Why is the characteristic time constant $\tau$ proportional to $R$?) [2 pts]

$$i = \frac{V_o - v_c}{R} = C \frac{dv_c}{dt}$$

$v_c$ will take longer to reach its final value if $R$ is increased because the current flowing through $R$ (to charge $C$) will decrease, hence it will take longer to deliver the charge $Q = CV_o$. 
Problem 1 (continued)
c) Assume that the circuit below is operating in steady state with the switch open for $t < 0$. Find and accurately sketch $v(t)$ for all $t$. [10 pts]

\[ t < 0: \]
\[ v(t < 0) = 5V \]
\[ v_i = 5mA \]
\[ i(t) = 5mA \]
\[ v(t = 0) = 0 \]
\[ v(t = \infty) = 0 \]

\[ t > 0: \]
\[ v(0^+) = -10V \]
\[ v(t) = 0 + [-10 - 0] e^{-t/1ms} = -10 e^{-1000t} \]

For $t < 0$: $v(t) = 5V$. For $t > 0$: $v(t) = -10 e^{-1000t}$
Problem 2: Semiconductor Materials and Devices [17 points in total]

a) Consider a Si sample maintained at \( T = 300 \text{K} \), uniformly doped with Arsenic atoms to a concentration \( 3 \times 10^{16} \text{cm}^{-3} \). The electron mobility = 1000 \( \text{cm}^2/V\text{s} \); hole mobility = 400 \( \text{cm}^2/V\text{s} \).

i) **Estimate** the resistivity of this sample. (Use \( q = 1.6 \times 10^{-19} \text{C} \) in your calculation.) [4 pts]

As is a Column V element \( \rightarrow \) donor in Si
\[
N_D = 3 \times 10^{16} \text{cm}^{-3}, \quad N_A = 0 \quad \Rightarrow \quad n = 3 \times 10^{16} \text{cm}^{-3}, \quad \rho = \frac{n_i^2}{n} \approx 3000 \quad \text{cm}^{-3}
\]

\[
\rho = \left[ q \mu_n n + q \mu_p p \right]^{-1} \approx \left[ q \mu_n n \right]^{-1} \quad \text{since} \quad n \gg p
\]

\[
\rho = \left[ 1.6 \times 10^{-19} \times 1000 \times 3 \times 10^{16} \right]^{-1} = \left[ 4.8 \right]^{-1} \approx 0.2 \Omega \text{-cm}
\]

resistivity \( \approx 0.2 \Omega \text{-cm} \)

ii) How will the resistivity of this sample change if it were to be doped additionally with \( 3 \times 10^{16} \text{cm}^{-3} \) Phosphorus atoms? [3 pts] carrier mobilities would be degraded

\( P \) is also a Column V element \( \rightarrow \) donor in Si since \( N_D + N_A \uparrow \)
\[
N_D = 6 \times 10^{16} \text{cm}^{-3}, \quad N_A = 0 \quad \Rightarrow \quad n = 6 \times 10^{16} \text{cm}^{-3}
\]

The resistivity will **decrease** (circle one)
by a factor that is **less than** (circle one) 2 when phosphorus is added because

the number of conduction electrons will double, but \( \mu_n \) will decrease

b) Explain (using 1 or 2 sentences) why a pn junction has capacitance. [2 pts]

A pn junction has capacitance because

charge is stored in the depletion region of a pn junction.

The width of the depletion region, and hence the charge stored, varies with the bias voltage. \( C_J \equiv \left| \frac{dQ}{dV_D} \right| \)
Problem 2 (continued)

c) Assume the diodes in the circuit below can be modeled as perfect rectifiers.

![Diode Circuit Diagram]

i) For what values of $V_{in}$ is D1 on? Explain your reasoning. [3 pts]

D1 is on for $V_{in} \geq 1$ Volt because

forward current can flow in D1 as long as $V_{in} > V_{out}$.

D2 fixes $V_{out}$ at 1V, unless $V_{in}$ causes $V_{out}$ to be $> 1$ Volt.

ii) For what values of $V_{in}$ is D2 on? Explain your reasoning. [2 pts]

D2 is on for $V_{in} < 2$ Volts because

if $V_{in}$ exceeds 2V, $V_{out}$ will exceed 1 Volt and D2 will be reverse biased. (If D2 is on for $V_{in} > 2V$, reverse current would have to flow in D2 - which cannot be.)

iii) Accurately plot $V_{out}$ vs. $V_{in}$ on the axes provided. [3 pts]

For $V_{in} < 2V$, D2 is on and so $V_{out}$ is fixed at 1V.

For $V_{in} > 2V$, D2 is off and so $V_{out} = \frac{1k\Omega}{1k\Omega + 1k\Omega} V_{in} = \frac{1}{2} V_{in}$
Problem 3: MOSFET and Common-Source Amplifier [17 points in total]

a) The following is the $i_D$-$V_{DS}$ characteristic of an n-channel MOSFET:

Indicate how this characteristic would change (by drawing the modified $i_D$-$V_{DS}$ characteristic with appropriate changes in $I_{DSAT}$ and $V_{DSAT}$):

i) when $V_T$ is lowered – use a labeled solid line on the plot above [2 pts]

\[ I_{DSAT} = k' \frac{W}{2L} (V_{GS} - V_T)^2 \text{ increases} \]

\[ V_{DSAT} = V_{GS} - V_T \text{ increases} \]

slopes at small $V_{DS}$ = $k' \frac{W}{L} (V_{GS} - V_T - \frac{V_{DS}}{2})$ increases

ii) when channel-length modulation is significant – use a labeled dashed line on the plot above [2 pts]

no change in $V_{DSAT}$, slope at small $V_{DS}$

slope in saturation region > 0

iii) when the current is limited by velocity saturation, rather than pinch-off – use a labeled dotted line on the plot above [2 pts]

\[ V_{DSAT} = \frac{L}{M} V_{Sat} < V_{GS} - V_T \text{ (decreases)} \]

$I_{DSAT}$ decreases

slope at small $V_{DS}$ unchanged
Problem 3 (continued)
b) Below to the left is the $i_D$ vs. $v_{DS}$ characteristic for a long n-channel MOSFET with $V_T = 1$ V.

![Graph of $i_D$ vs. $v_{DS}$]

What is $V_{GS}$? [2 pts]

$$V_{DSAT} = V_{GS} - V_T$$

$$3 = V_{GS} - 1 \quad \Rightarrow \quad V_{GS} = 4 \text{ V}$$

$$V_{GS} = 4 \text{ Volts}$$

c) Suppose the MOSFET in part (b) is used in the amplifier circuit shown above to the right.

i) Draw the load line on the MOSFET $i_D$-$v_{DS}$ plot (above to the left). [3 pts]

ii) In what region is the MOSFET operating? [2 pts]

The MOSFET is operating in the [linear, saturation, cutoff] (circle one) region because

$$v_{DS} > V_{DSAT} \text{ and } i_D > 0$$

iii) What is the incremental change in the output voltage (i.e. $v_{out}$) for a -1 mV change in the input voltage (i.e. $v_{gs} = -1$ mV)? [4 pts]

$$i_{DSAT} = k' \frac{W}{2L} (V_{GS} - V_T)^2 = 1 \text{ mA}$$

$$\Rightarrow k' \frac{W}{2L} (3)^2 = 1 \text{ mA}$$

$$k' \frac{W}{2L} = \frac{2}{9} \text{ mA/V}^2$$

$$v_{out} = -g_m v_{gs} (5 \text{ kΩ})$$

$$= -\frac{2}{9} \times 10^{-3} (-10^{-3})(5 \times 10^3)$$

$$v_{out} = 3.3 \text{ mV}$$

Small-signal equivalent circuit:

$$g_m = \frac{\partial i_D}{\partial v_{gs}} = \frac{\partial}{\partial v_{gs}} \left[ k' \frac{W}{2L} (V_{GS} - V_T)^2 \right]$$

$$= k' \frac{W}{2L} (V_{GS} - V_T)$$

$$= \frac{2}{9} \frac{\text{mA}}{\text{V}^2} \times 3 \text{V} = \frac{2}{3} \text{ mS}$$