FINAL

Name: _____

SID: _____

Problem	Score
1	
2	
3	
4	
5	
Total (of 100)	

- **3 pages of handwritten notes, double sided, 8.5 by 11 inches**
- **Mark all results with a box.**
- Write solutions on the exam sheets. No extra pages.
- Simplify algebraic results as much as possible.
- Show derivations and explain briefly how you arrived at your result.

1. [20 points] In Figure 1, $C_s = 1\text{pF}$, $C_f = 6\text{pF}$, $C_L = 1\text{pF}$, $C_x = 300\text{fF}$.
   a) Calculate the dynamic settling time for 1% relative error. Assume that the transconductor is ideal with value $G_m = 1\text{mS}$. Assume that all capacitors have been discharged before an input is applied to the circuit.
   Note: the feedforward current through C_f has significant effect on the solution.
   b) Now the transconductor in Figure 1 is realized with the circuit shown in Figure 2. Assume that both transistors operate in the forward active region with $g_{m1} = g_{m2} = 2\text{mS}$ and ignore all parasitics and capacitors except those explicitly shown in the diagrams. Find the maximum value of C_y that results in a phase margin (for stability) of 75 degrees.

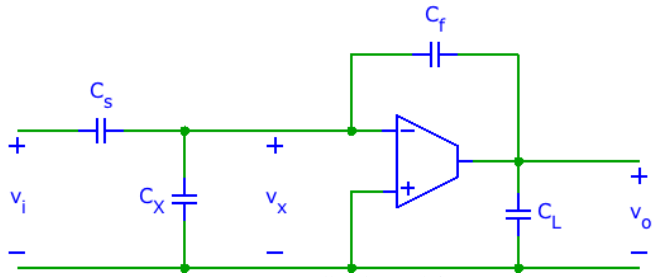


Figure 1 Feedback amplifier.

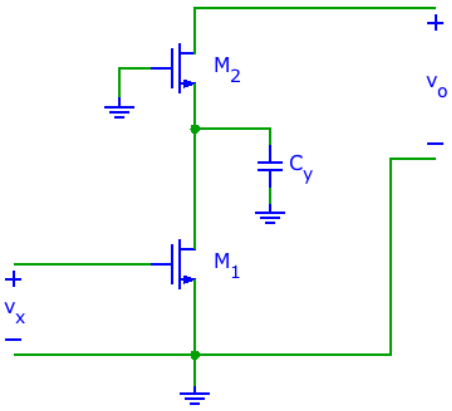


Figure 2 Transconductance amplifier.

2. [20 points] The total noise at the output of the SC filter shown in Figure 3 is $\sqrt{\overline{v_{oT}^2}} = 6\mu V$ rms.

   a) Modify the filter such that $\sqrt{\overline{v_{oT}^2}} = 3\mu V$ without changing the frequency response of the filter. Report the new component values in the Table below.

   b) By what approximate factor does the power of the new filter increase compared to the original design?

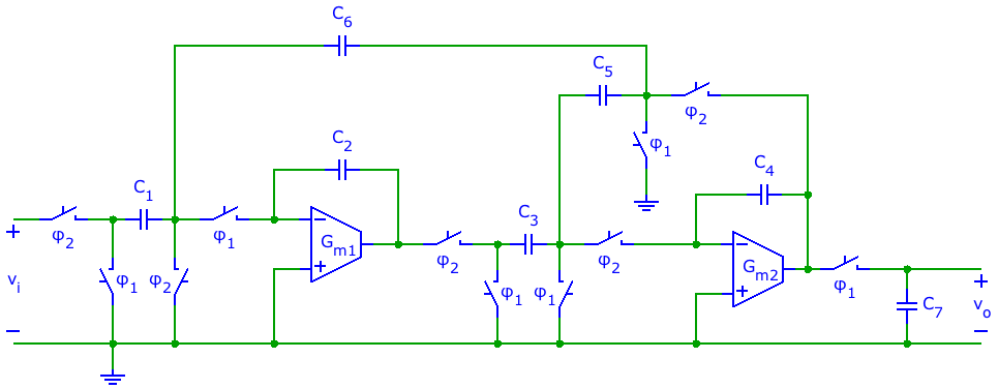
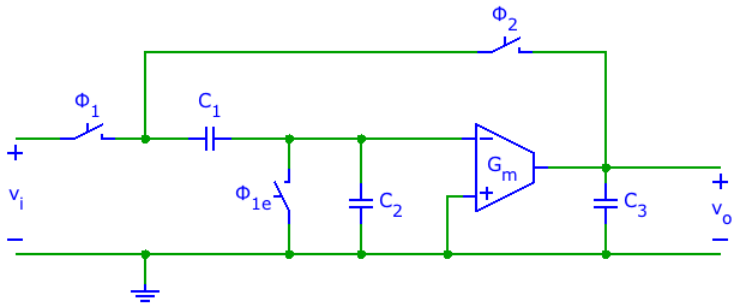


Figure 3 Switched capacitor filter.

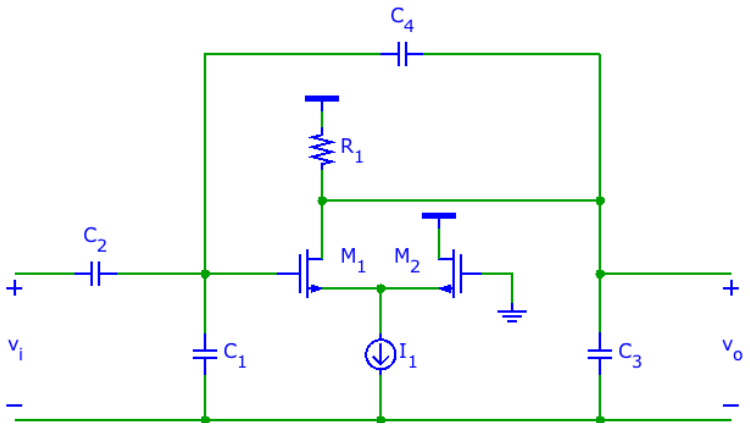
Component	Original Value	New Value
C_1	3pF	
C_2	2pF	
C_3	1pF	
C_4	5pF	
C_5	1pF	
C_6	2pF	
C_7	4pF	
G_{m1}	4mS	
G_{m2}	2mS	

3. [20 points] The circuit shown below is controlled by an f_s=200MHz non-overlapping two-phase clock.
   a) Calculate the value of G_m required for a dynamic setting error of 0.02%.
   b) Calculate the rms noise voltage at the output of the circuit at the end of phase 2. Assume that the transconductor is realized with a transistor amplifier with $\gamma = 0.8$ and $\alpha = 2.5$. Include the noise from both clock phases!

   Parameter: $C_1 = 1\text{pF}, C_2 = 200\text{fF}, C_3 = 2\text{pF}$. The switch on-resistance contributes negligible to the dynamics of the circuit. Assume that the clock has a 50% duty cycle and ignore the clock non-overlap time.



4. [20 points] For the circuit below, find the minimum value of I_1 that results in no more than 5ns slewing time for a 1V step input. Assume that the circuit changes abruptly from slewing to linear settling and that the low-frequency gain is large and that the charge on the capacitors has been properly initialized before the step is applied.
   Parameter: $C_1 = 200\text{fF}, C_2 = 1\text{pF}, C_3 = 2\text{pF}, C_4 = 300\text{fF}, V_1^* = V_2^* = 100\text{mV}$.



5. [20 points] For the circuit below, determine the flicker noise corner frequency required such that flicker noise adds no more than 20% to the total noise power at v_o in the band from 1Hz to infinity. Assume M_1 is biased in the forward active region and neglect flicker noise at frequencies higher than the bandwidth of the circuit.
   Parameter: low frequency gain $A_{vo} = v_o/v_i = -2$, $R_L = 5\text{k}\Omega$, $C_L = 200\text{fF}$, $\gamma = 0.8$.