

**UNIVERSITY OF CALIFORNIA**  
**College of Engineering**  
**Department of Electrical Engineering and Computer Sciences**

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**Midterm**  
**Thursday, March 12, 2009**

**EECS 240**  
**SPRING 2009**

*You should write your results on the exam sheets only. Partial credit will be given only if you show your work and reasoning clearly.*

**Name:** Solutions

**SID:** \_\_\_\_\_

**Problem 1** \_\_\_\_\_ / 13

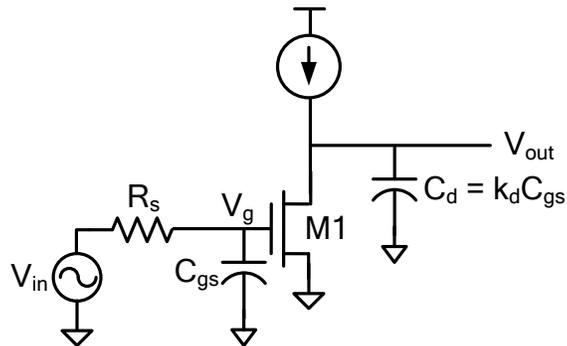
**Problem 2** \_\_\_\_\_ / 10

**Problem 3** \_\_\_\_\_ / 9

**Total** \_\_\_\_\_ / 32

### Problem 1 (13 points) Capacitance and SNR

In this problem we will look at optimizing the SNR of the amplifier shown below.



You should use the following assumptions and simplifications to solve this problem:

- The input of the amplifier ( $V_{in}$ ) is a sinusoid with an angular frequency of  $\omega_{in}$  and an amplitude of  $A_{in}$ .
- The transistor is biased with a fixed  $V^*$  so that its gain ( $g_m r_o$ ) is  $A_{v0}$ .
- Assume  $R_s$  is noiseless, and ignore all capacitors except those shown in the figure.
- You should assume that  $1/(r_o C_d) \gg \omega_{in}$ . In other words,  $V_{out}(j\omega_{in})/V_g(j\omega_{in}) = A_{v0}$ .
- Your final answers should be a function of only  $k$ ,  $T$ ,  $\gamma$ ,  $\omega_{in}$ ,  $A_{in}$ ,  $k_d$ ,  $A_{v0}$ ,  $R_s$ , and  $C_{gs}$ .

a) (4 pts) What is the voltage noise variance  $\overline{v_{on}^2}$  at the output of the amplifier?

No noise from  $R_s$ , so just look at output node:

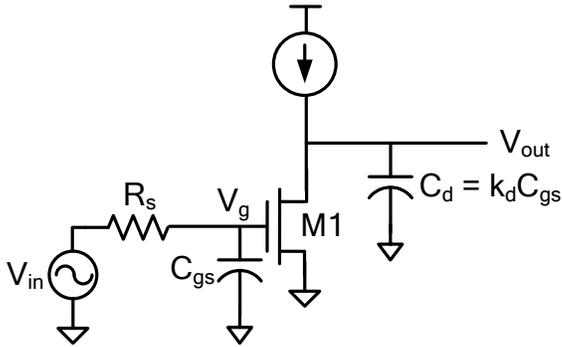


$$\overline{v_{on}^2} = 4kT \gamma g_m \cdot r_o^2 \cdot \frac{1}{4r_o C_d}$$

$$\overline{v_{on}^2} = \frac{kT}{C_d} \cdot \gamma A_{v0}$$

$$\boxed{\overline{v_{on}^2} = \frac{kT}{C_{gs}} \cdot \frac{\gamma A_{v0}}{k_d}}$$

- b) (4 pts) What is the mean-squared signal voltage  $\overline{V_{out}^2}$  at the output of the amplifier?



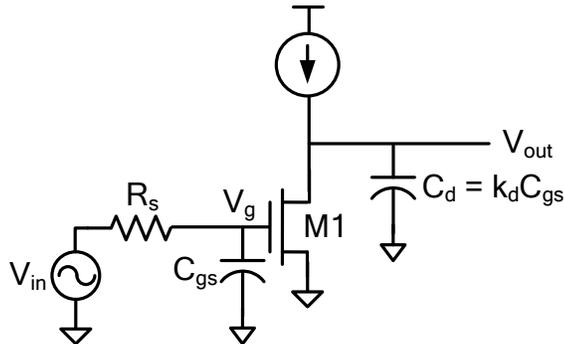
$$\frac{V_g(s)}{V_{in}(s)} = \frac{1}{1 + s R_s C_{gs}}$$

$$\left| \frac{V_g(j\omega_{in})}{V_{in}(j\omega_{in})} \right|^2 = \frac{1}{1 + \omega_{in}^2 R_s^2 C_{gs}^2}$$

$$V_{out} = A_{vo} V_g \quad \overline{V_{in}^2} = \frac{A_{in}^2}{2}$$

$$\overline{V_{out}^2} = A_{vo}^2 \frac{A_{in}^2}{2} \cdot \frac{1}{1 + \omega_{in}^2 R_s^2 C_{gs}^2}$$

- c) (5 pts) Keeping the  $V^*$  of the transistor fixed, what value of  $C_{gs}$  maximizes the SNR  $\overline{V_{out}^2} / \overline{v_{on}^2}$  at the output of the amplifier?



$$\frac{\overline{V_{out}^2}}{\overline{v_{on}^2}} = \frac{A_{vo}^2 \cdot A_{in}^2 / 2}{(1 + w_{in}^2 R_s^2 C_{gs}^2)} \cdot \frac{C_{gs}}{kT} \cdot \frac{k_d}{\delta A_{vo}}$$

$$SNR \propto \frac{C_{gs}}{1 + w_{in}^2 R_s^2 C_{gs}^2} \quad (A_{vo} \text{ doesn't change with } C_{gs} \text{ since } V^* \text{ is fixed})$$

$$\frac{\partial SNR}{\partial C_{gs}} = \frac{(1 + w_{in}^2 R_s^2 C_{gs}^2) - 2 C_{gs} w_{in}^2 R_s^2 C_{gs}}{(1 + w_{in}^2 R_s^2 C_{gs}^2)^2} = 0$$

$$1 + w_{in}^2 R_s^2 C_{gs}^2 = 2 w_{in}^2 R_s^2 C_{gs}^2$$

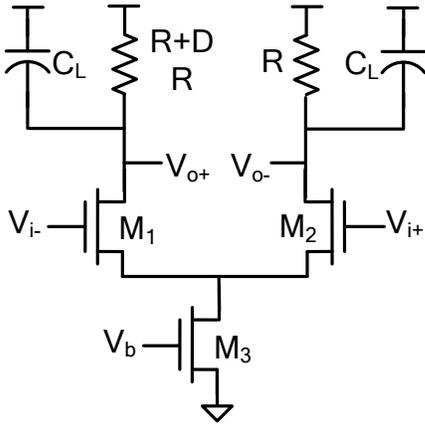
$$w_{in}^2 R_s^2 C_{gs}^2 = 1$$

$$C_{gs} = \frac{1}{w_{in} R_s}$$

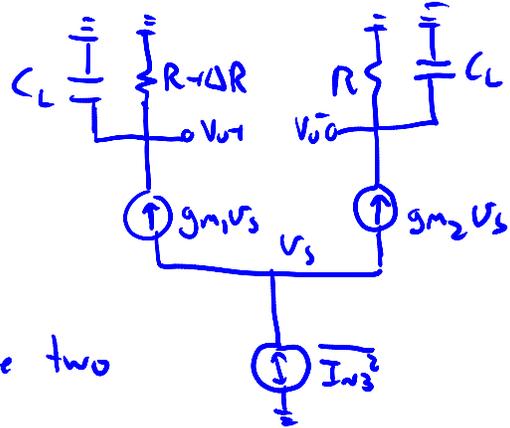
$$(i.e., w_{in} = \frac{1}{R_s C_{gs,opt}})$$

## Problem 2 (10 points) Noise

Considering only the noise current from  $M_3$ , what is the variance of the differential voltage noise at the output of the amplifier shown below? You can ignore all the  $r_o$ 's of the transistors and all capacitors except those explicitly drawn in the schematic. You can assume that  $M_1$  and  $M_2$  are identical (i.e.,  $g_{m1} = g_{m2}$ ), and you should provide your answers in terms of  $k$ ,  $T$ ,  $\gamma$ ,  $C_L$ ,  $(g_{m3}/g_{m1})$ ,  $(\Delta R/R)$ , and  $A_{v,nom} = (g_{m1}R)$ .



Noise model:



$I_{n3}$  splits equally between the two sides since  $g_{m1} = g_{m2}$ . So:

$$V_{o+} = \frac{I_{n3}}{2} \cdot \frac{R + \Delta R}{1 + s(R + \Delta R)C_L}$$

$$V_{o-} = \frac{I_{n3}}{2} \cdot \frac{R}{1 + sRC_L}$$

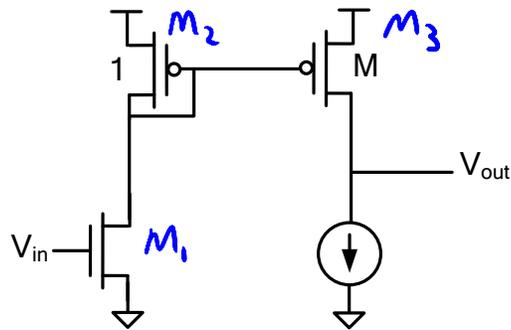
$$V_{o,diff} = V_{o+} - V_{o-} = \frac{I_{n3}}{2} \cdot \frac{(R + \Delta R)(1 + sRC_L) - R(1 + s(R + \Delta R)C_L)}{(1 + s(R + \Delta R)C_L)(1 + sRC_L)}$$

$$\frac{V_{o,diff}}{I_{n3}} = \frac{\Delta R/2}{s^2 R(R + \Delta R)C_L^2 + sRC_L(2 + \frac{\Delta R}{R}) + 1}$$

$$\begin{aligned} \text{So: } \overline{V_{o,diff}^2} &= 4kT \gamma g_{m3} \cdot \frac{\Delta R^2}{4} \cdot \frac{1}{4RC_L(2 + \frac{\Delta R}{R})} \\ &= \frac{kT}{C_L} \cdot \frac{\gamma}{4} \cdot g_{m3} \Delta R \cdot \frac{\Delta R/R}{2 + \Delta R/R} \end{aligned}$$

$$\overline{V_{o,diff}^2} = \frac{kT}{C_L} \cdot \frac{\gamma A_{v,nom}}{4} \cdot \left(\frac{g_{m3}}{g_{m1}}\right) \cdot \frac{(\Delta R/R)^2}{(2 + \Delta R/R)}$$

**Problem 3 (9 points) Amplifier Design**



- a) (4 pts) Assuming that the  $V_n^*$  of the NMOS and PMOS transistors are  $V_n^*$  and  $V_p^*$  respectively and ignoring the  $r_o$  of all of the transistors, what is the nf of the amplifier shown above? In other words, relative to the noise current from the input transistor, what is the noise current density that flows into the amplifier's output? You should provide your answer in terms of  $V_n^*$ ,  $V_p^*$ , and  $M$ .

$$i_{n,tot}^2 = i_{n,m1}^2 \cdot M^2 + i_{n,m2}^2 \cdot M^2 + i_{n,m3}^2$$

$$nf = \frac{i_{n,tot}^2}{i_{n,m1}^2 \cdot M^2} = 1 + \frac{i_{n,m2}^2}{i_{n,m1}^2} + \frac{i_{n,m3}^2}{i_{n,m1}^2 \cdot M^2}$$

$$\overline{i_{n,m1}^2} = 4kT \delta g_{m1} \Delta f$$

$$g_{m1} = 2I_0 / V_n^*$$

$$\overline{i_{n,m2}^2} = 4kT \delta g_{m2} \Delta f$$

$$g_{m2} = 2I_0 / V_p^*$$

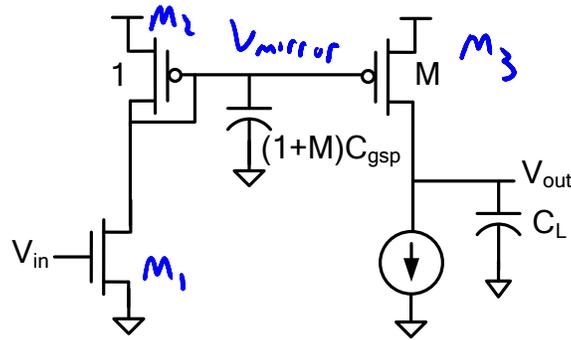
$$\overline{i_{n,m3}^2} = 4kT \delta g_{m3} \Delta f$$

$$g_{m3} = M g_{m2}$$

So:

$$nf = 1 + \frac{g_{m2}}{g_{m1}} + \frac{M g_{m2}}{M^2 g_{m1}}$$

$$nf = 1 + \left(1 + \frac{1}{M}\right) \cdot \frac{V_n^*}{V_p^*}$$



- b) (5 pts) Now let's look at the stability of this amplifier under feedback using the model shown above (ignore the  $r_o$ 's and all capacitors except the ones shown in the model). If the amplifier is placed into unity-gain feedback with a closed-loop bandwidth of  $\omega_{gbw}$ , what is the maximum  $M$  that will provide at least  $45^\circ$  of phase margin? You should provide your answer in terms of  $\omega_{gbw}$  and the  $\omega_T$  of the PMOS transistors.

$$\text{Pole at } V_{\text{mirror}}: \omega_{p2} = \frac{g_{m2}}{(1+M)C_{gs2}} = \frac{\omega_T}{(1+M)}$$

$\omega_{p2}$  is the new-dominant pole.

Dominant pole crosses over at  $\omega_{gbw} (= \frac{g_{m1}}{C_L})$

For  $\geq 45^\circ$  phase margin, want:

$$\omega_{p2} \geq \omega_{gbw}$$

$$\frac{\omega_T}{1+M} \geq \omega_{gbw}$$

$$\boxed{M \leq \frac{\omega_T}{\omega_{gbw}} - 1}$$