Solutions for Midterm #1 - EECS 145M Spring 2008

1 Successive-approximation A/D converter operation
(1) set all bits zero, and bit counter i = N
(2) set bit i to one
(3) send all bits to D/A converter, output = V_0
(4) Use comparator to compare input V_1 and D/A output V_0
(5) if $V_1 < V_0$ set bit i to zero
(6) decrease bit counter: i = i −1
(7) loop back to step (2) until all bits have been determined
See Figures 3.16 and 3.17 on page 169 of the textbook
[3 points off for not describing how the binary search is done]
[3 points off for not including the D/A converter or comparator- you cannot directly compare an analog input with a digital value]

2.1
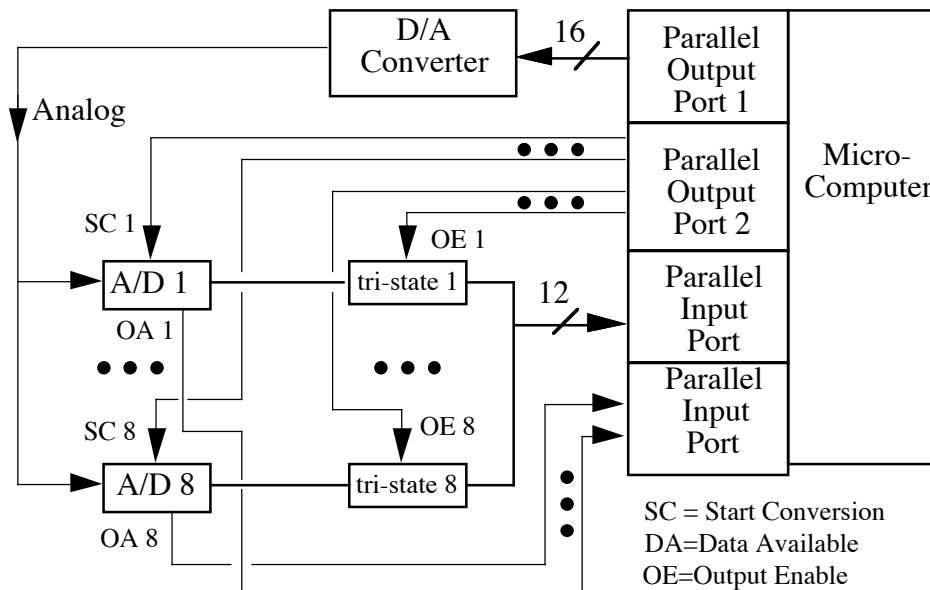
The following are essential [3 points off for each omitted]:
- Connect the analog output of the D/A to the analog inputs of all A/Ds
  Note: S/H amplifiers are not needed since the D/A can provide the hold
- Connect the 12 bit A/Ds to separate tri-state drivers
- Connect the outputs of the tri-state drivers together to form a data bus (can't input 8 x 12 bits in parallel)
- Connect the data bus to 12 bits of the parallel input port
- Provide 8 separate output port lines for initiating conversion of the 8 A/Ds (could be combined with next signal)

- Provide 8 separate output port lines for enabling the 8 separate tri-state drivers (this was essential)
- Provide input for 8 separate input port lines to indicate when individual A/Ds have completed conversion

2.2 The steps needed to measure the first transition voltage V(0,1) for the first A/D converter.

1   set SC1 low, disable all tri-state drivers, set N = 0 (16 bits)
2   Put N on D/A
3   wait 10μs until D/A has settled [using wait(10)]
4   Put low-high edge on SC1 output line to start conversion
5   Wait until output data available
6   enable tri-state 1 (disable all others)
7   read input port to get value M
8   Put high-low edge on SC1 output port to end conversion cycle
9   if M=0, increase N by one and loop back to step 2
10 If M=1, save (D/A voltage step)(N-1/2) as the transition voltage
    [3 points off for writing to D/A and reading a value from A/D but not determining V(0,1)]

2.3 Send successive 16-bit numbers 0 to $2^{16}-1$ to the D/A converter and convert the analog output with the A/D. Whenever the A/D output value changes, store the corresponding D/A value in a transition voltage table

Determine the D/A values corresponding to first and last A/D transition voltages, and the equation of the line that passes through them. **Linearity** is a measure of how closely the other measured transition values pass through the line.
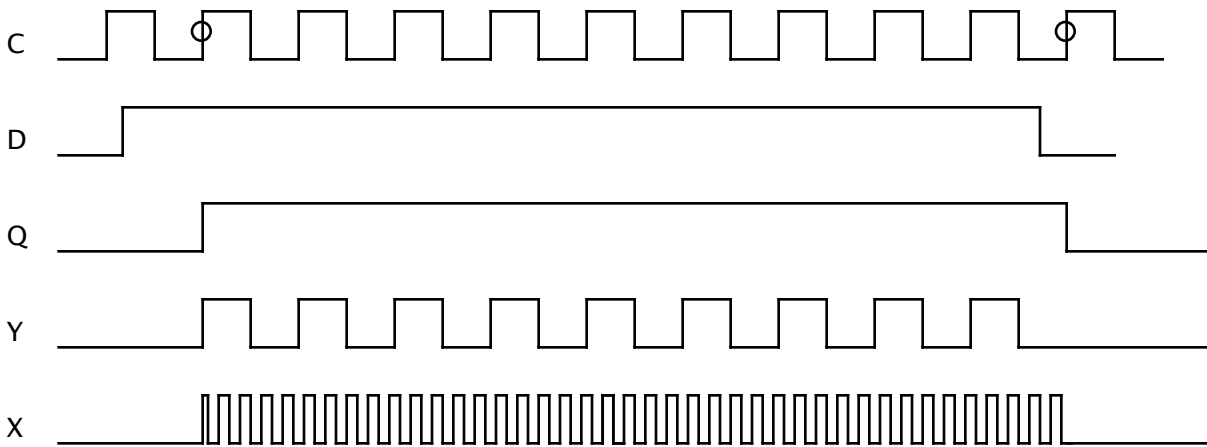
[2 points off for determining maximum differential linearity or maximum absolute accuracy]

2.4 The method can determine the A/D accuracies to 1/16 LSB (±1/32 LSB was OK).

Note that 1 A/D LSB = 16 D/A LSBs.

[5 points off for an answer of 1/2 or 1 A/D LSB]

3.1

[2 points off if C does not show comparator pulses at frequency f]

[2 points off if D does not show the 1-second pulse]

[2 points off if Q goes high when D goes high rather than on the next edge of C after D goes high]

[2 points off if Q goes low when D goes low rather than on the next edge of C after D goes low]

Note 1: the rising and falling edges of Q are controlled by the rising edges of C which clocks D onto Q

Note 2: counter 1 is controlled by Q, not D

[2 points off if X does not show 100 MHz pulses while Q is high]

[2 points off if Y does not show comparator pulses while Q is high]

[2 points off if any pulses are shown on X and Y when Q is low]

3.2

1) Reset counters

2) Assert D high

3) Wait approximately 1 second

4) Assert D low

5) Wait for Q to go low [go to step 1) if 1-second measurement requirement is exceeded]

6) Read counters 1 and 2

7) Compute $f = f_{pulser} *$ counter2 / counter1

8) Cycle back to 1) to take another measurement of f.

[2 points off for not waiting for Q to go low before reading the counters- counter 1 keeps running until Q goes low]

[4 points off if calculation or formula for f is not given]

[2 points off if calculation of f does not depend on value of f_{pulser}]

[Making D low, reading counter 1 until it reaches 100 million, and taking counter 2 as the frequency was not accepted for full credit because the accuracy of this approach is much poorer than what the circuit is capable of doing]

3.3

Since the designed called for a measurement of f every second, the minimum frequency is 1 Hz.

The highest frequency is given by the frequency limit of counter 2, which is 100 MHz

3.4
Since the edges on C and the 100 MHz pulses are not synchronized, counter 1 could vary by one count from measurement to measurement even if the input frequency did not change. So the uncertainty in counter 1 is 1 part in 100 million. There is no uncertainty in counter 2 – all pulses are counted exactly.

At 1 Hz the uncertainty is 10^{-8} Hz
At 100 MHz, the uncertainty is 1 Hz

EECS145M Midterm #1 class statistics:

Problem	max	average	rms
1	10	7.5	2.7
2	45	35.6	7.9
3	45	34.1	7.0
total	100	77.2	13.5

Grade distribution:

Range	number	*approximate letter grade*
40-49	2	F
50-59	0	D
60-69	2	C
70-79	2	B
81-89	10	A–, B+
90-99	1	A
100	0	A+