#### MIDTERM EXAM NAME \_\_\_\_\_\_ March 18, 2010

#### **INSTRUCTIONS**

- Read all of the instructions and all of the questions before beginning the exam.
- There are 4 problems on this midterm exam, totaling 100 points. The tentative credit for each part is given to help you allocate your time accordingly. You have a total of 1 hour and 30 minutes to finish this exam. Be careful not to spend all your time on any one part.
- This is a closed book exam, except you can have one two-sided  $8.5'' \times 11''$  sheet of notes.
- Unless otherwise noted on a particular problem, you must show your work (in the space provided plus the backs of the pages) for all problems to receive full credit; *simply providing answers will result in only partial or no credit, even if the answers are correct.* If you require extra space beyond what is provided, be sure to turn in any material that is required to support your solutions. Note that there are extra pages at the end of this exam. Do not use any attached pages until you have exhausted the pages contained in this exam.
- Turn in the entire exam, including this cover sheet.
- Put your name on every page of this exam, as well as on any additional material that you submit.
- Be sure to provide units where necessary.

Signature:

Total:	/ 100 points
Problem 4:	/ 18 points
Problem 3:	/ 20 points
Problem 2:	/ 33 points
Problem 1:	/ 29 points

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#### **<u>Problem 1</u>**. Total 29 points

Please provide short written answers to the questions that follow.

(a) Would you expect the resolution of lithography over a metal layer to be better or worse than over a silicon dioxide layer? Why?

(b) Would you expect oxidation to be faster or slower over <111> silicon when compared with <100> silicon? Why?

(c) You've just done a standard photoresist spin & bake, lithography, and etch step using a *per-fectly anisotropic* RIE. However, the sidewalls of the etched film are not straight. What is most likely causing this? What can you do to fix this in your next fabrication run?

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#### Problem 1. (continued)

- (d) Which of the following are true for a reactive ion etch (RIE) using the surface inhibitor mechanism? Circle the letters for all that apply.
  - a. Oxygen is always added to the etch chemistry in order to remove polymer.
  - b. High energy ions physically remove the film to be etched.
  - c. Neutral radicals are the dominant etchants.
  - d. Polymer protects the sidewalls from etching.
  - e. Electric fields are used to direct the primary etchants to sites to be preferentially etched in order to achieve an anisotropic etch.
- (e) List three reasons why a 5X-reduction stepper projection lithography system might be preferred over a contact lithography system.

(f) List two reasons why a contact lithography system might be preferred over a stepper projection lithography system.

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Problem 2.

The cross-section of a polysilicon-oxide-silicon substrate sandwich structure with a photoresist pattern on top is shown. The pattern will be etched via RIE. You can assume that the etch is 100% anisotropic; that the selectivity of silicon (and polysilicon):SiO<sub>2</sub>:photoresist = 2:1:1; and that the etch rate of silicon (and polysilicon) is 0.1  $\mu$ m/min. Carefully draw cross-sections of the structure to the left of the dotted line after (a) 2 minutes of etching; (b) 5 minutes of etching; and (c) 11 minutes of etching. Be sure to specify relevant angles and dimensions for each cross-section. Also, for each case use dotted lines to indicate where the *original* photoresist and wafer surfaces were before *any* etching.



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**<u>Problem 2</u>**. (continued)

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<u>Problem 2</u>. (continued)

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#### **<u>Problem 3.</u>** Total 20 points

The structure shown below has gone through the following process steps:

- i) Start with a bare  $\langle 100 \rangle$  silicon wafer.
- ii) Grow 300 nm of oxide.
- iii) Deposit 100 nm of Si<sub>3</sub>N<sub>4</sub>.
- iv) Lithography: Mask 1.
- v) Etch 100 nm of  $Si_3N_4$  and *m* nm of  $SiO_2$ .
- vi) Remove PR.
- vii) Wet oxidation @ 1000°C for t minutes.

Determine *t* and *m*.



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<u>Problem 3</u>. (continued)

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#### **<u>Problem 4.</u>** Total 18 points

You are given the layout below along with the process traveler to follow. In the layout, each box corresponds to  $1 \ \mu m^2$ . In the mask legend, cf = "clear field" and df = "dark field". In the process traveler, assume that all lithography steps use positive photoresist, and that all etch steps are 100% selective to the intended film. Also, assume that RIE etches are anisotropic, but any other type of etch has some degree of isotropy. Finally, assume that hydrofluoric acid etches silicon dioxide (of any type) at the rate of 300 nm/min.



#### Process Traveler:

Note that steps i) through xxiv) are exactly as in the standard LOCOS-isolated NMOS process covered in lecture.

- i) Silicon oxidation: target = 100nm.
- ii) LPCVD  $Si_3N_4$ : target = 100nm.
- iii) Lithography: Mask I (active area).
- iv) Dry etch  $Si_3N_4$  to clear it in field areas.
- v) Field isolation implant: B+ (p-type).
- vi) Remove PR.
- vii) Grow 1µm of SiO<sub>2</sub> by thermal oxidation (LOCOS oxidation).
- viii) Blanket etch all Si<sub>3</sub>N<sub>4</sub> in hot phosphoric acid wet etchant.
- ix) Threshold voltage implant: B+ (no mask).
- x) Remove 100nm of damaged oxide via a timed wet etch in hydrofluoric acid (HF).
- xi) Grow 100nm of gate thermal oxide in an ultra-clean furnace.
- xii) LPCVD situ phosphorous-doped gate polysilicon: target = 400 nm.
- xiii) Lithography: Mask II (gate polysilicon).
- xiv) Dry etch polysilicon to clear the field areas.
- xv) Remove PR.
- xvi) D/S ion implantation: As (n-type).

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#### Problem 4. (continued)

- xvii) Oxidize a bit (10nm) and anneal at 1050°C to activate dopants and drive-in diffusion.
- xviii) LPCVD PSG: target =  $1\mu m$ .
- xix) Reflow PSG (& a little bit of diffusion) at 950°C.
- xx) Lithography: Mask III (contact hole).
- xxi) Dry/wet etch  $SiO_2$  down to n+ S/D regions.
- xxii) Sputter Al: target = 500nm.
- xxiii) Lithography: Mask IV (metal).
- xxiv) Dry etch Al to clear the field areas.

Here's where things start to differ from standard LOCOS-isolated NMOS.

- xxv) Lithography: Mask V (release).
- xxvi) Dip in hydrofluoric acid for 10 minutes.
- xxvii) Remove PR.

#### Instructions:

Draw the cross-section along the A-A' axis at the end of this process, giving important vertical and lateral dimensions.

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<u>Extra Page</u>.

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**Possibly Useful Data:** 

