

Problem 1

(a) E-Beam lithography has to address and expose the pixels in a serial fashion. Optical lithography can expose all pixels simultaneously by flood exposure (a parallel process). The later has a higher throughput.

(b)

(i) AZ1350J is a positive resist .Kodak 747 is a negative resist.

(ii) For positive resist (AZ1350J), $\gamma = \frac{1}{\log_{10}(90/45)} = 3.32$

For negative resist (Kodak 747), $\gamma = \frac{1}{\log_{10}(12/7)} = 4.27$ (higher resist contrast)

(iii) Resist Kodak 747 (better sensitivity) only needs 12mJ/cm2 to fully exposure while AZ13750J requires 90 mj/cm2 to fully expose.

(c)Technology factors: $k_1 = 0.58$ and $k_2 = 0.54$

$$L_{\min} = k_1 \times 248\text{nm} / 0.5 = \mathbf{0.28 \mu\text{m}}$$

$$\text{DOF} = k_2 \times 248\text{nm} / (0.5)^2 = \mathbf{0.53\mu\text{m}}$$

(d) Steppers maintained at constant temperature to minimize thermal run-in/out overlay errors due to different thermal expansion coefficients of mask and substrate.

(e) To reduce difference of standing wave's I_{\max} and I_{\min} , one can use a resist with absorption dyes or by placing an antireflection coating on the reflecting interface.

Problem 2

(a) $C_T(\text{SiH}_4) = 0.02 \times 4.8 \times 10^{18} = 9.6 \times 10^{16}$ molecules/cm³

Since 1 molecule of SiCl₄ gives 1 Si atom and the growth rate is assumed to mass-transfer limited,

$$\therefore \frac{dy}{dt} = \frac{1}{\left(\frac{1}{k_s} + \frac{1}{h_G}\right)} \cdot \frac{C_T}{5 \times 10^{22}} \approx \frac{h_G C_T}{5 \times 10^{22}} = \frac{2.62 \times 9.6 \times 10^{16}}{5 \times 10^{22}} = 5.03 \times 10^{-6} \text{cm/sec} = \mathbf{503 \text{ \AA/sec}}$$

(b) (i) We will use the linear regime of the curve where surface-reaction mechanism determines the growth rate R

$$R = \text{constant} \times \exp[-E_a/kT] \text{ or } E_a = -1000 \text{ k} \times \frac{\ln R(1) - \ln R(2)}{1000/T(1) - 1000/T(2)}$$

$R = 0.2 \mu\text{m/min}$ at $1000/T = 0.93$ and $R = 0.01 \mu\text{m/min}$ at $1000/T = 1.1$

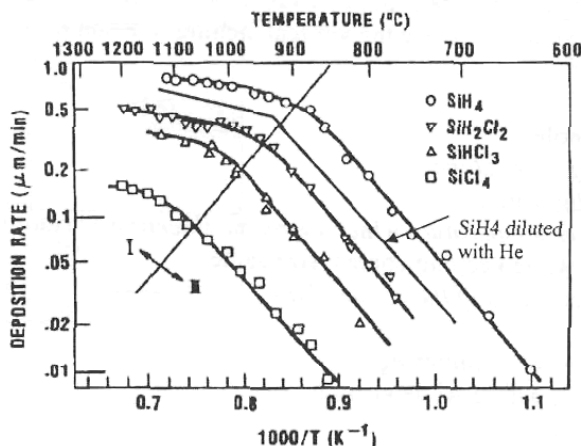
$$\text{Therefore } E_a = -1000 \times 8.617 \times 10^{-5} \times \frac{\ln(0.2) - \ln(0.01)}{0.93 - 1.1} = \mathbf{1.5\text{eV}}$$

(ii) The SiH₄ concentration C_T is lower due to the lower partial pressure of SiH₄. Therefore R will lower for both mass transfer and surface reaction limited regions

The k_s term is not affected by the dilution effect.

The h_G term ($= D/\bar{\delta}$) will have no change in D ($\propto \frac{T^{3/2}}{P}$) because P_{total} is same. The $\bar{\delta}$ term $= \frac{2L}{3\sqrt{\frac{\rho UL}{\mu}}}$ will

have minor changes in density and viscosity due to He dilution but will be second-order.

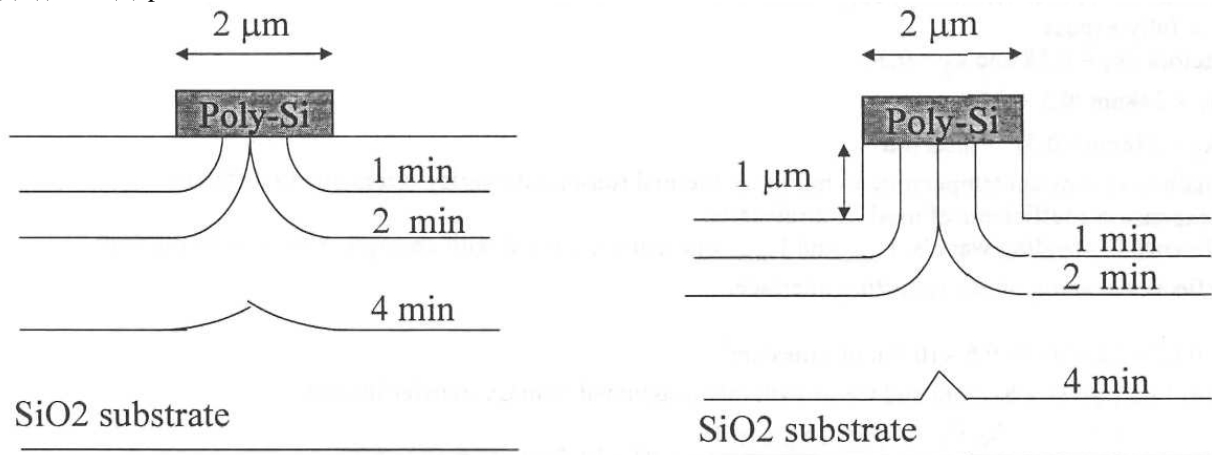


(c) (i) Step coverage problem is due to directional flux used for deposition (e.g. sputtering). Since the spherical receiving surface will be making different angles to the wafer surface for different r positions, we will still see step coverage effects.

- (ii) Flux arriving at wafer distance r $F' \propto (\cos \theta)^2 / r^2$
 Thickness deposited on wafer $\propto F' \times \cos \Phi$ (with $\Phi = \theta$) $\propto (\cos \theta)^3 / r^2$
 Since $\cos \theta = (r/2)/R$, therefore **thickness** $\propto r$.

Problem 3

(a) (i) and (ii) profiles :



(iii)

(A) At release time = 2 min, Method (ii) has a larger gap of clearance than Method (i). Less stiction problem to release the beam.

(B) For a given required clearance, Method (ii) takes less wet etch time

(C) The larger cleared gap between $t = 2$ to 4 min can assist the HF etch solution to give more vertical etching component above the spike regions, giving a slightly more planar substrate surface.

(b) Overetch fraction time over step $\Delta = 7000/4000 = 1.75$

$$\text{Worst-case etching time } t = \frac{h_f}{v_f} \times \frac{(1 + \delta)(1 + \Delta)}{(1 - \Phi_f)} = \frac{h_f}{v_f} [(1 + 0.03)(1 + 1.75)/(1 - 0.05)] = \frac{h_f}{v_f} \times 2.98$$

$$\text{Mask erosion } W/2 = v_m \times \cot \theta \times t$$

$$\text{Minimum etching selectivity of poly-Si to mask } S_{\text{im}} = \frac{v_f}{v_m} = \frac{4000}{1000/2} [\cot 80^\circ] \times 2.98 = 4.2$$

(c) (i) O_2 addition to CF_4 plasma will generate more F^* radical which will etch Si faster. This chemical etching component is isotropic in nature.

(ii) Substrate bombardment by vertically directed energetic ions can sputter away deposited polymer and also damage the substrate atoms at bottom area. Both effects will increase the vertical etching rate compared with the lateral sidewall etching rate.

Problem 4

(a) ___+___ Use a wet chemical etch for the contact holes

Explanation: Wet etch is isotropic. Contact hole has gentler slope.

___+___ Increase substrate temperature **during** Al deposition

Explanation: Surface diffusion is enhanced with higher temperature which evens out thickness variation.

___-___ Thicken the oxide around the contact holes while keeping contact size same

Explanation: More shadowing effect with higher aspect ratio of the contact hole

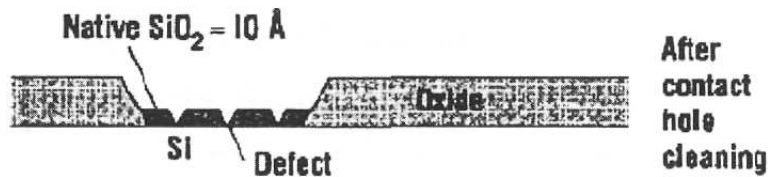
___+___ Develop a CVD Al process

Explanation: CVD is more conformal than evaporation and sputtering

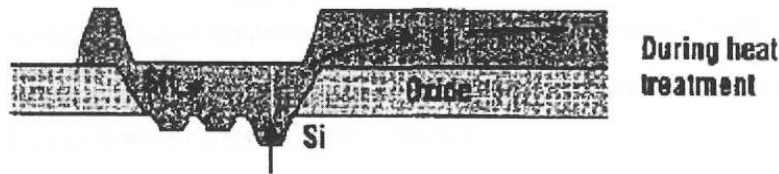
___+___ Fill the contact hole with CVD tungsten plug before Al deposition

Explanation: The W plug will planarize the contact hole

(b) (i) Dissolution of Si into Al is easier at regions with localized "defects" (e.g. pinholes in the residual native oxide left by contact hole cleaning or Al grain boundaries). The localized Al-Si reactions will form spikes instead of a uniform interfacial reaction.



(ii) Perimeter of contact holes is closer to the Al interconnect which has a length much larger than the contact hole size. The volume of Al in the interconnect acts like a large reservoir to induce more Si dissolution. Therefore the spikes forms near the perimeter region will be larger and deeper.



(iii) If the Al spike has a depth deeper than the junction depth (e.g. source/drain of a MOSFET), it will form a Schottky ohmic contact with the p-type substrate, shorting the source/drain contact to substrate.

(c) Al-Cu alloy during the sintering step at 400C will precipitate out at the grain boundaries of the interconnect, blocking the grain boundary diffusion paths for the electromigrated Al atoms. MTF will improve.

(d) Key ideas of dual damascene process flow: 2 layers of dielectrics → contact via patterning → interconnect patterning (larger than contact via size) → Cu deposition → planarized by CMP.

To improve the process latitude and performance, one can add etch stops between dielectric layers, encapsulate all copper by depositing diffusion barrier films before Cu deposition which can also serve as a seed layer for Cu plating if copper plating is used.

