Problem 1 Lab Questions (20 points total)

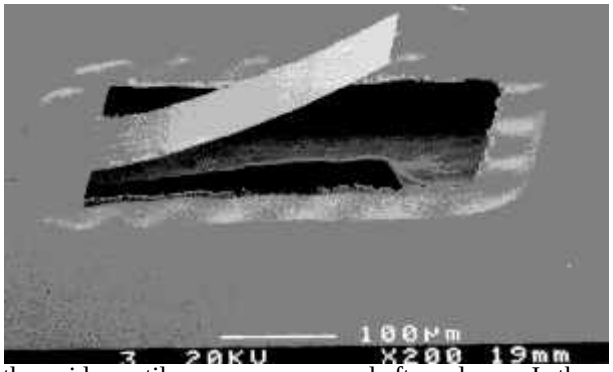
(a) (3 points) In our EE143 lab, we use Phosphorus for the source and drain diffusion. However, most advanced processes use Arsenic. What is the advantage of using Arsenic ? Why we are limited to phosphorus as the S/D doping source in the EE143 lab?

(b) (3 points) Why is a 4-point probe measurement of sheet resistance better than that of a 2-point probe? Explain with a diagram illustrating the operation principle of a 4-point probe measurement.

(c) (4 points) The Lab MOSFET devices have W_{mask}(drawn width on the mask)=100μm, and L_{mask} (drawn channel length on the mask) varying from 100μm to 5μm . If we apply 0.1V to the drain of each device and a large bias voltage to the gates (for example, V_G =+5V), sketch the ratio V_D/I_D versus L_{mask}. What is the intercept of this plot with the horizontal axis (L_{mask} axis)?

Problem 1 Lab questions continued

(d) (6 points) The following scanning electron microscopy (SEM) picture shows the cantilever structure of the MEMS chip after XeF2 etching.



(i) Explain why the oxide cantilever curves upward after release. Is the oxide cantilever under compressive or tensile stress **before** release?

(ii) The Si substrate is not flat after XeF2 etching. Explain why the Si region directly underneath the oxide cantilever is elevated. [Hint: Sketch the time progression of the etching profiles]

(e) (4 points) What is a SALICIDE process ? Make a list of additional equipments we will need in the EE143 Lab to implement the SALICIDE process.

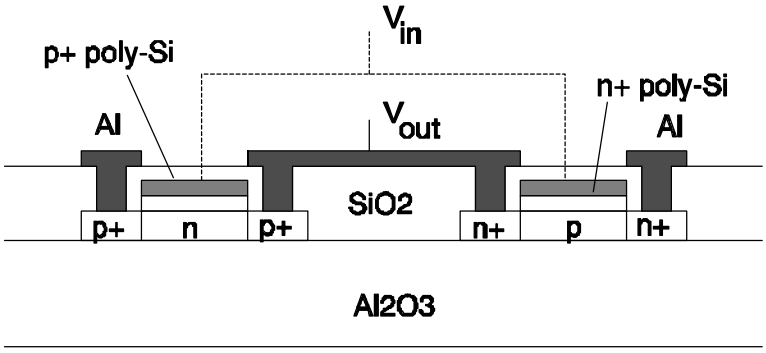
Problem 2 General Questions (20 points total)

(a) (4 points) How will the Short Channel Effect of MOSFETs (i.e., V_T **decreases** when channel length L decreases) be affected by :

(i) Increasing the substrate doping concentration

(ii) Decreasing the gate oxide thickness.

(b) (6 points) The following cross-section shows a CMOS inverter fabricated with silicon-on-sapphire (SOS) technology. Sapphire (Al_2O_3) is a perfect insulator. If we choose to use this technology. Explain how **three** of our EECS143 MOS layout design rules can be changed (larger or smaller). Justify your explanations.



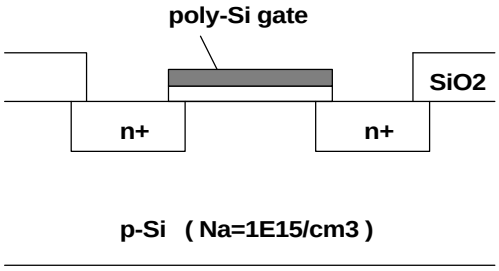
Rule1

Rule 2

Rule 3

Problem 2 General Questions continued

(c) (4 points) You are faced with the following three choices for forming the source and drain of a NMOS transistor.



(i) Shallow predeposition of Q phosphorus atoms /unit area , followed by a drive-in at 1100°C for 60 minutes.
(ii) Shallow predeposition of Q phosphorus atoms /unit area , followed by a drive-in at 1150°C for 30 minutes.
(iii) Implantation of Q phosphorus atoms / unit area to a R_p of 0.3μm, followed by an anneal at 950°C for 10 minutes.[For simplicity, let us ignore the lateral straggle ΔR_t associated with ion implantation in this problem]

Use the following diffusivity values:

TEMPERATURE	D(Phosphorus)
950°C	5×10^{-5} μm^2 / min
1100°C	2×10^{-3} μm^2 / min
1150°C	5×10^{-3} μm^2 / min

(A) Which process will give the shortest MOSFET channel length L ? Justify your answer.

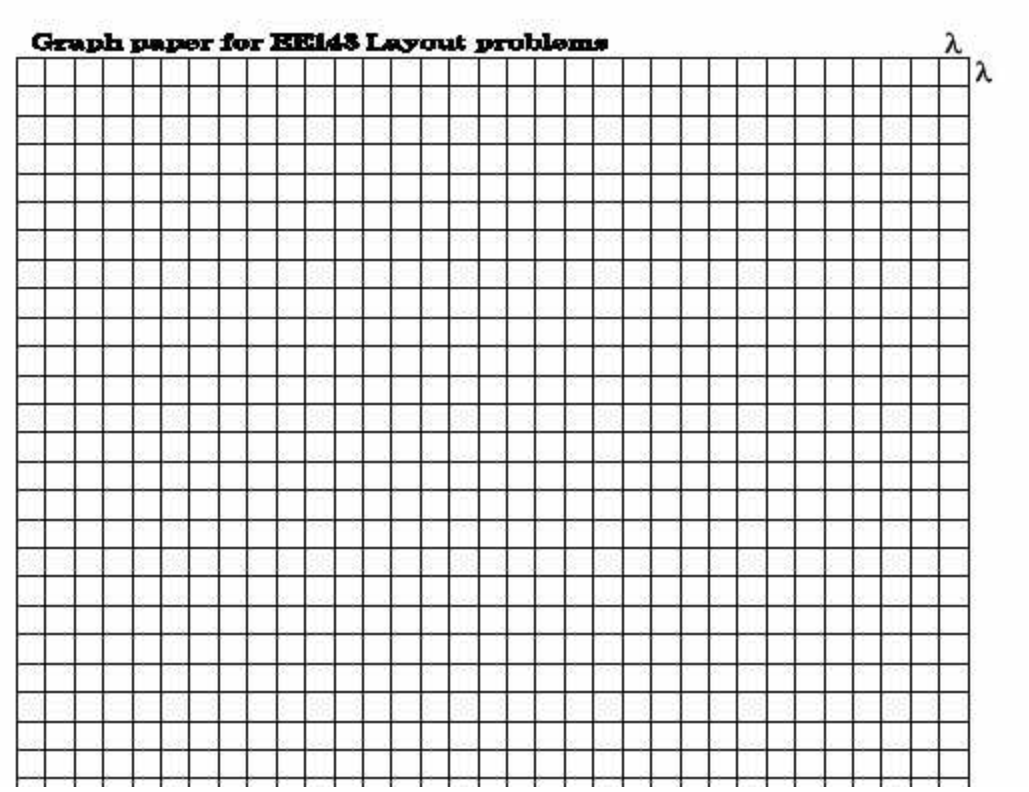
(B) If the substrate doping is increased from 1×10^{15} to 1×10^{16} boron atoms /cm^3 , which of the three processes will exhibit the greatest change in channel length ?

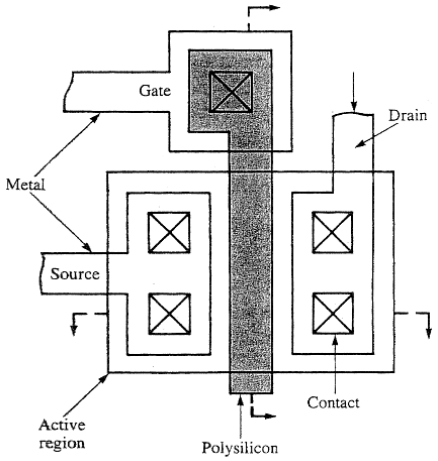
(d) (3 points) What is electromigration failure for interconnects ? How do we improvement the electromigration reliability of interconnects ?

(e) (3 points) Explain why n+ shallow junctions are easier to fabricate than p+ shallow junctions.

Problem 3 Layout (15 points total)

(a) (10 points) The following layout of a MOSFET has L=2 λ and W= 8 λ. Use the graph paper provided to layout a minimum-size transistor. Label the design rules you used.



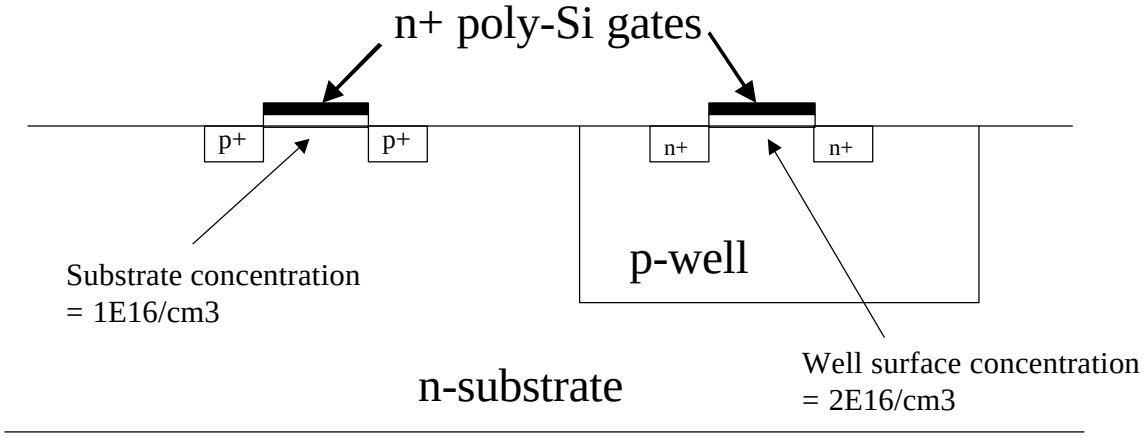


(b) (3 points) With Aluminum as the contact metal, what is the advantage of using two (or more) smaller-size contact holes instead of one larger-size contact hole.

(c) (2 points) An integrated circuits usually has MOSFETs with many various L, and W values, If reactive ion etching is used to pattern the contact holes, it is preferable to layout many identical-size contact holes within the S/D regions instead of a single large one. What is the reason?

Problem 5 MOS (25 points total)

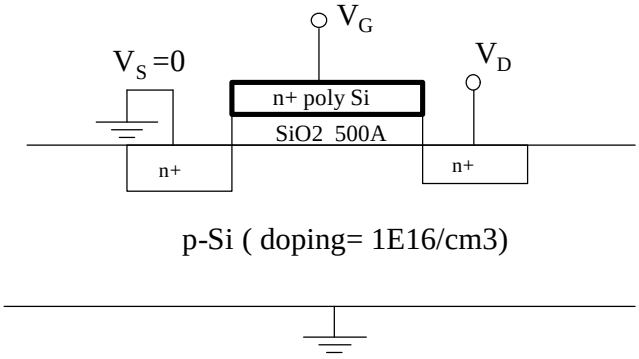
(a) (10 points)A p-well CMOS process uses n^+ poly as the gate material for both the n and p channel devices. The gate oxide thickness is 220 Å with no oxide or interface charge. The n-substrate has a doping concentration of 10^{16}/ cm^3 and the p-well has a doping concentration of 2×10^{16}/ cm^3 near the surface region.



Our design goal is to make $V_{TN} = - V_{TP}$ with a blanket threshold implant step for both the n and p channel devices. **Determine the implant dopant specie AND the required implant dose**.

Problem 5 MOS continued

(b)The following figure shows a NMOS with n+ poly gate, gate oxide thickness = 500 Å, and a p-substrate with doping concentration = 1E16/cm^3.



(i) (6 points) If there is no oxide or oxide interface charge, calculate the threshold voltage V_T for V_D =0.

(ii) (3 points) Calculate the drain current for $V_G = V_D = 3$ volts. Use k =50 μA / V^2.
Note: I_{DS} (triode region) = k [$(V_G - V_T) V_{DS} - V_{DS}^2 /2$] ; I_{DS} (saturation region)=k[$(V_G-V_T)^2/2$]

(iii) (3 points) After exposing the MOSFET to cosmic radiation which creates an oxide interface charge Q_f, the threshold voltage shifts upward by +8 volts [i.e., ΔV_T = +8 volts]. Determine the **sign and magnitude** of Q_f .

(iv) (3 points) What is the drain current for $V_G = V_D = 3$ volts after the MOSFET is exposed to cosmic radiation ?

Problem 6 Mechanical Stress in thin films (10 points total)

A 500 μm -thick bare Si wafer originally has a radius of curvature of +300 m.
(Given: ν_{Si}= 0.272, E_{Si} = 1.9 x 10^{11}Newton/m^2 ,

RADIUS OF CURVATURE RELATIONSHIP : $\sigma_f = \frac{E_s \times t_s^2}{(1-\nu)_s \times 6 \times r \times t_f}$)

(a) (4 points) A 3000 Å oxide film is deposited onto the Si wafer. After oxide deposition, the wafer radius is measured to be +200 m. Calculate the stress of the oxide film. Is the oxide stress compressive or tensile?

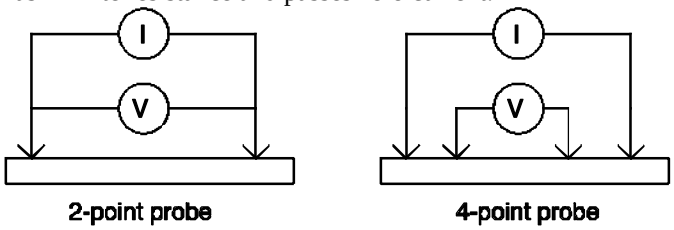
(a) (6 points) A 6000 Å nitride film is then deposited on top of the oxide and the wafer radius of curvature becomes +240 m. Calculate (i) the total stress of the oxide/nitride dual layer and (ii) the stress of the nitride film alone. Is the nitride stress compressive or tensile?

EE143 S2000 Final Exam Sample Solutions

Problem1 Lab Questions

(a) As diffuses slower than P. It is easier to make shallower junctions.
As has higher solid solubility. The higher surface concentration gives lower contact resistance.
We are using phosphorus SOG in the lab mainly for safety reasons (arsenic is toxic!).

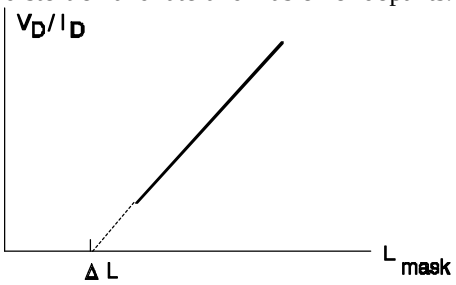
(b) The 2-point probe measurement will include voltage drops caused by the current source between probes and the voltmeter, and contact resistance. The 4-point probe method do not include this voltage drops because the voltmeter has infinite resistance and passes zero current.



(c) For small V_D and $V_G > V_T$, MOSFET is in linear region

$I_D = \mu C_{ox} \frac{W}{L_{eff}} (V_G - V_T) V_D$

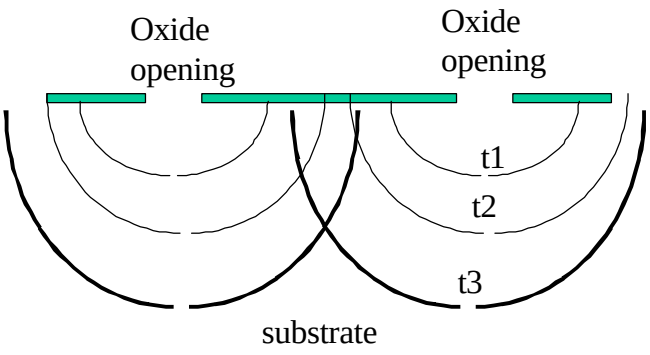
$\frac{V_D}{I_D} = \frac{L_{mask} - \Delta L}{W \mu_n C_{ox}(V_G - V_T)}$, the plot will give the intercept ΔL on the x-axis which is due to processing distortion and lateral diffusion of dopants.



(d)

(i) The cantilever beam is mainly field oxide with a small poly pattern near the anchor boundary.
Explanation 1 : The top part oxide is under tensile stress and the bottom part of oxide under compressive stress.
Explanation 2 : The oxide is under comrpresive stress and the poly pattern is under tensile stress.

(ii) Schematic showing time development of XeF2 etching profiles

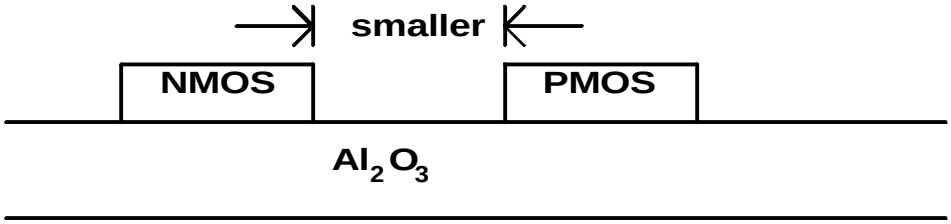


(e) SALICIDE
An oxide spacer is created by anisotropic RIE between the poly gate and S/D region. Blanket metal (e.g. Ti) is deposited. Annealing will give $TiSi_2$ on the poly gate and S/D regions but puree Ti will remain at the oxide spacer region. Selective chemical etch can remove the Ti.
Advantages: (1) The $TiSi_2$ has metallic conductivity. The gate and S/D will all have low sheet resistance (< 1 ohm/square) as compared with ~50 ohm/square for heavily doped poly and Si. This increases the circuit speed because of lower parasitic resistances. (2) This is a self-aligned process. No additional lithography step is needed for oxide spacer and the metal formation.
List of additional quipment needed in 143 Lab:
(i) We need CVD reactor for oxide deposition
(ii) Reactive ion etcher to etch spacer
(iii) Metal deposition system (sputtering machine) for Ti deposition
(iv) Ion Implanter for S/D doping
(v) Rapid Thermal annealing furnace (optional) (i) We need CVD reactor for oxide deposition

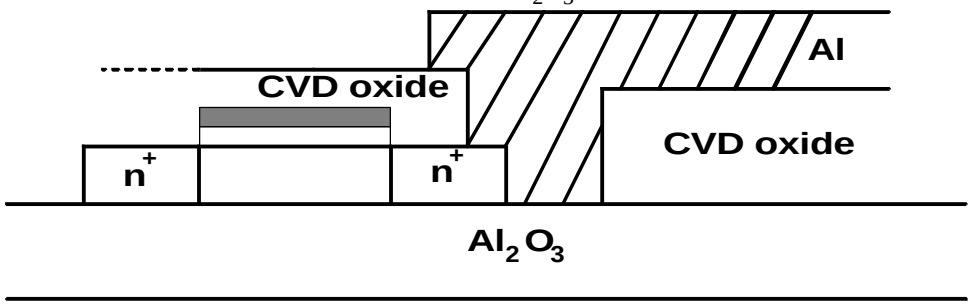
Problem2 General Questions

(a) (i) Increasing substrate concentration will decrease both x_{dmax} and junction depth x_j. Both reductions will reduce lateral depletion charges underneath the gate contributed by the S/D junctions. Therefore less short channel effect.
(ii) Reducing gate oxide thickness has no effect according to the Yau model especially when VD is small. [Optional answer (more advanced) : The vertical electric field created by the gate is larger when oxide is thinner. The lateral electric field contributed by the S/D junctions is relatively less. Therefore less short channel effect , especially for larger VD bias.

(b)
Rule 1 Min thin-oxide to thin-oxide spacing can be reduced for SOS, the substrate is insulating (Al_2O_3). No field oxide is required for device isolation.



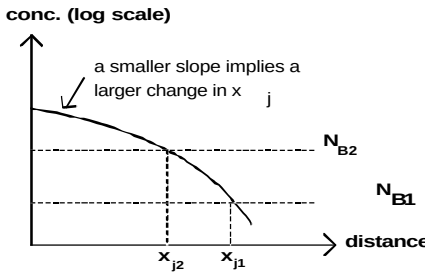
Rule 2 Minimum underlap of contact in thin oxide can be reduced because the substrate is insulating. Misalignment on contact cut will not create a short on Al_2O_3.



Rule 3 Minimum metal - metal spacing can be reduced. There is no field oxide bird's beak. The MOS islands can be made very thin. Therefore wafer topography is flatter.

If you have other reasonable explanations, they are acceptable.

(c)



(A) $\sqrt{Dt}$ of (ii) $> \sqrt{Dt}$ of (i) $> \sqrt{Dt}$ (iii)

$\therefore$ (ii) has the largest lateral diffusion

$\therefore$ Process(ii) gives shortest MOSFET channel.

(B)

Since the dose Q is the same, a lager $\sqrt{Dt}$ implies a smaller slope (i.e., more dopant spread-out)

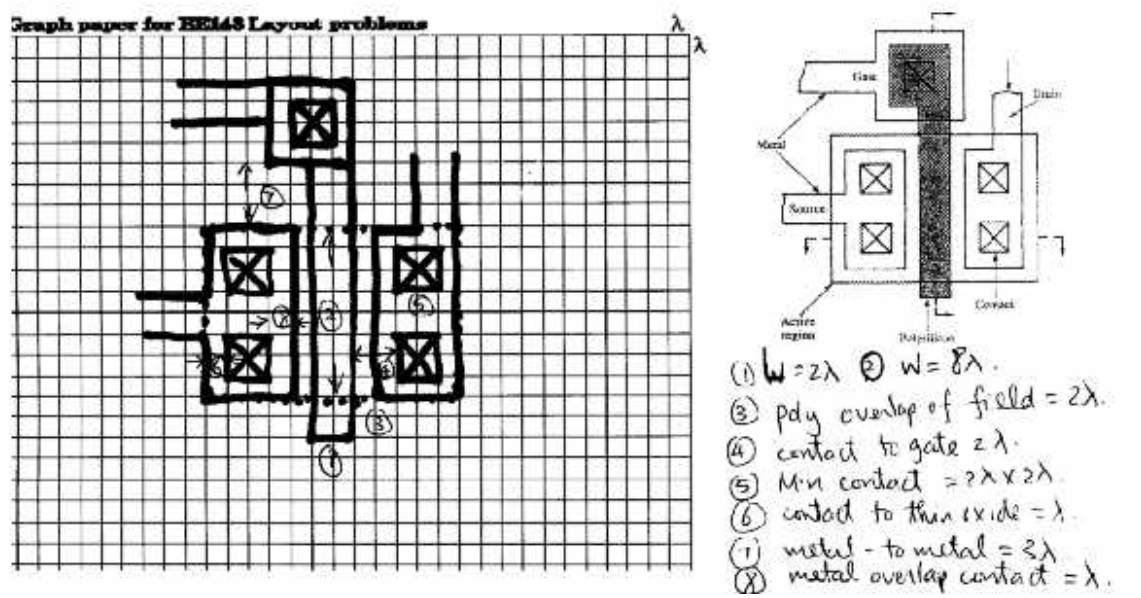
$\therefore$ Process (ii) gives the greatest change in channel length

(d)Electron flux will transfer momentum to interconnect lattice atoms, creating atomic motions laong direction of electron low. When there is a local divergence of the atomic flux (e.g. unequal grain boundary diffusion paths) , mass accumulation (formation of hillocks) or mass depletion (formation of voids) can occur. There can lead to shorting of neighboring interconnects or complete open of an interconnect. The common practice to improve interconnect reliability is to create alloying precipitates (e.g. Al-Cu) along the grain boundaries which block grain boundary diffusion.

(e) n+ junction are using phosphorus or arsenic dopants as implantation species. Both have larger mass compared with boron which is used for p+ junctions. The heavier mass is easier to create amorphous substrate layer which give less channeling effect. Diffusivities of P and As are also slower than that of Boron, giving shallower junctions.

[Optional answers: A higher implant voltage can be used for P and As for the same Rp – no compromise on throughput due to beamline implanter currenmt drop. TED for P and As is less than that of Boron.]

Problem3 Layout



b) Al spiking , if occurs, will have shallower spikes if contact holes are smaller (less supply of Al)
c) Etching rates are more uniform with an array of identical contact holes (less loading effect variation)

Problem 5 MOS

(a) $C_{ox}=1.57\times10^{-7}$ F/cm^2

$|\phi_n|$ =0.35V

$|\phi_p|$ =0.37V

With $N_a=10^{16}$/cm^3 and $N_d=2\times10^{16}$/cm^3

$$V_{TN} = -0.55+|\phi_p|+\frac{\sqrt{4\varepsilon_s qN_a|\phi_p|}}{C_{ox}} = +0.26V$$

$$V_{TP} = -0.55 - |\phi_n| - \frac{\sqrt{4\varepsilon_s qN_a|\phi_n|}}{C_{ox}} = -1.21V$$

$\therefore \Delta V_T = (-V_{TP}-V_{TN})/2 = +0.475V$

To make $V_{TN} = -V_{TP}$ =0.73V, we need a threshold implant of **boron** with a dose

$$\phi = \frac{\Delta V_T \times C_{ox}}{q} = 4.7\times10^{11}/\text{cm}^2$$

(a) $C_{ox}=6.9\times10^{-8}$ F/cm^2

$|\phi_p|$ =0.35V

$V_{FB} = -(0.55+|\phi_p|) = -0.90V$

With $N_a=10^{16}$/cm^3

$$V_{TN} = -0.55+|\phi_p|+\frac{\sqrt{4\varepsilon_s qN_a|\phi_p|}}{C_{ox}} = +0.50V$$

(b) $V_G - V_T = 3 - 0.5 < V_D$ =3V. Transistor is in saturation mode.

$I_{Dsat} = k[(V_G-V_T)^2/2] = 0.156$mA

(c) A negative Q_f will shift the V_T for more positive values.

+8V = $|Q_f|/C_{ox}$ implies $Q_f = -3.45\times10^{12}$ q / cm^2

(d) $V_G < V_T$. Transistor is in cutoff mode. $I_D \sim 0$.

Problem 6 MEMS

$$\sigma_f = \frac{E_s \times t_s^2}{(1-\nu)_s \times 6 \times r \times t_f}$$

(i) With the oxide deposited, the oxide stress is **compressive** since r changes from 300m to 200m (Si wafer more curved)

$t_f = 3 \times 10^{-7}$ m

$t_s = 5 \times 10^{-4}$m

$$\sigma_f \text{ (oxide)} = \frac{1.9 \times 10^{12} \times 25 \times 10^{-8}}{(1-0.272) \times 6 \times 3 \times 10^{-7}} \left(\frac{1}{300} - \frac{1}{200}\right) = -6.05 \times 10^{8} \text{ N/m}^2$$

(ii) With both the nitride and the oxide deposited, the wafer is less curved than with oxide alone . Therefore, the nitride film has a **tensile** stress. However, the total stress of the dual films is still **compressive** since r = 240 m and is still smaller than the original curvature of 300 m.

Now,

t_f (total) $= 9 \times 10^{-7}$ m

$$\sigma_f \text{ (dual film)} = \frac{1.9 \times 10^{12} \times 25 \times 10^{-8}}{(1-0.272) \times 6 \times 9 \times 10^{-7}} \left(\frac{1}{300} - \frac{1}{240}\right) = -1.0 \times 10^{8} \text{ N/m}^2$$

(iii) The stress due to the nitride alone is ~ $(-1.0 - (-6.05)) \times 10^8 \sim 5 \times 10^8$ N /m ^{2}(**tensile**)