Family Name _______________________  First name __________________________

Signature________________________________________________________________

Instructions: DO ALL WORK ON EXAM PAGES
This is a 90-minute exam (closed book).

Grading: To obtain full credit, show correct units and algebraic sign in answers.
Numerical answers which are orders of magnitude off will receive no partial credit.

Problem 1 (30 points) _____________

Problem 2 (30 points) _____________

Problem 3 (40 points) _____________

TOTAL (100 points) _______________
Problem 1 (30 points total)
We would like to implement a simple RC low-pass filter in integrated circuits. The top view, the equivalent circuit, and the cross-section along line AB are shown below. Design a process flow starting with p-substrate. We will use local oxidation (LOCOS) for device isolation [Consult the 143 reader or lecture notes for the LOCOS process]. The poly-Si is deposited by chemical vapor deposition with no dopant incorporated. In subsequent processing steps, the resistor region of the poly-Si is lightly doped (n⁻) while the capacitor region of the poly-Si is heavily doped (n⁺). You must show cross-sections along AB after each lithography step.

Process Description
1) Starting Material- lightly doped p-Si

Cross-Section along A-B
Problem 1 continued

Process Description

Cross-Section along A-B
Problem 2 Implantation and diffusion (30 points total)
The following schematic shows the process to form a planarized SiO$_2$ trench with a deep implant to form the channel stop at the bottom of the SiO$_2$-filled trench and junction isolation at the bottom of an n-well:

![Schematic Diagram](image_url)

(a) (3 points) For a final SiO$_2$ thickness of 0.5 µm, find the required etched Si thickness X.

(b) We will assume the SiO$_2$ has identical ion stopping properties as Si and the Si$_3$N$_4$ is infinitely thin. The boron implantation (dose = $1 \times 10^{13}$/cm$^2$) was performed such that the boron pr peaks exactly at the bottom of the SiO$_2$-filled trench.

(i) Use implantation range tables/figures to find out the required implanter accelerating voltage in kV if:

(A) (3 points) B$^+$ ions are used.

(B) (4 points) BF$_2^+$ ions are used. [Hint: B mass = 11 amu, F mass = 19 amu]

(ii) (10 points) The n-Si substrate has a background doping concentration $N_B = 1 \times 10^{15}$/cm$^3$. Calculate the junction depth $x_{j1}$ between the buried implant p-layer and the surface n-Si. [x=0 at surface]
Problem 2 continued

(iii) (5 points) Use the Irvin’s curves to determine the sheet resistance of the Si in regions \textbf{under} the SiO$_2$ trench.

(iv) (5 points) Use a solid line to sketch qualitatively the boron concentration versus depth under the boron implantation (using the same energy as part (i) ) was performed \textbf{before} Explain the differences.
Problem 3 Short Questions (40 points total)
(a) (10 points) Explain why minimum resolution and depth of focus requirements cannot be optimized simultaneously by using shorter wavelength photons for projection optical lithography.

(b)(10 points) The linear coefficients of expansion of the photolithography mask material and Si wafers are $8 \times 10^{-6}/\degree C$ and $2.3 \times 10^{-6}/\degree C$ respectively. For a 1X projection printer, the mask temperature can vary by $\pm 1\degree C$. The wafer temperature is independent of the mask temperature and can also vary by $\pm 1\degree C$. Calculate the maximum thermal run-out of the alignment marks near the edge of the wafer (diameter =
(c) (10 points) Photoresist lines often show variation of widths when they are patterned over steps with highly reflective surface. To minimize this linewidth variation, an anti-reflective coating (ARC) of polymer is spun on the substrate prior to the application of the resist. The attached figure shows the cross-section when we want to pattern an aluminum line running across a substrate step. Discuss two mechanisms with which the ARC will help to minimize the

(d) (10 points) For a particular oxidation process, it is known that the oxidation rate $\frac{dx}{dt}$ is 0.24 m/hour when the oxide thickness is 0.5 µm and 0.08 m/hour when the oxide thickness is 1 m. Find the linear oxidation constant (B/A) and the parabolic oxidation constant B. Give answers in proper units.
Problem 1

Process Description

1) Starting wafer, p- Si

2) Pad oxide growth
   Si₃N₄ deposition
   Active area patterning (Mask #1)
   Channel stop Boron implantation
   Remove photoresist

3) Local oxidation to grow field oxide
   Strip Si₃N₄
   Strip pad oxide (chemical dip)

4) As implantation to form n⁺ in active region
   Gate oxide oxidation

5) Undoped poly-Si deposition
   Blanket As implant (low dose) to form n⁻ poly-Si

6) Masking resistor region with photoresist
   (Mask #2)
   As implantation (high dose) to form n⁺poly-Si

7) Pattern poly-Si (Mask #3)
   Deposit CVD SiO₂
   Diffuse and activate dopants in poly-Si with short
   time annealing (= 900°C)

8) Metal contact opening (Mask #4)
9) Al deposition
Al interconnect patterning (Mask #5)

General Comments:

**Problem 1:**

0) *Always avoid unnecessary lithography steps.*

1) One should *always* do lightly doped region and then convert it to heavily doped if needed. If you count on compensation to convert n⁺ to n⁻, you may not have the precision to control the net concentration. For example, the n⁺ poly-Si has donor concentration $= 10^{20}$/cm$^3$. To convert it to n⁻ poly-Si with net donor concentration $= 10^{15}$/cm$^3$, we need 0.99999 x $10^{20}$/cm$^3$ acceptor concentration (1 part in $10^5$ precision !)

2) One should not implant through the gate oxide with a high dose implantation (e.g. to form the n⁺ capacitor bottom plate). Here, the dose used is approx $10^{15}$/cm$^2$. It will damage the gate oxide integrity which lies directly on top of the active device region. This practice is somewhat tolerable for low-dose threshold implants (dose $\approx 10^{11}$/cm$^2$). In the case of source and drain implants (high dose), you can implant through an overlying thin oxide because the source/drain is outside the gate oxide area;

To be sure, you should always do the implant before growing the gate oxide if that is possible.

3) One can pattern the poly-Si before doping or vice versa. Either way is acceptable in this midterm exam. However, it is advisable to dope the poly-Si first because the photoresist will be lying on flatter topography and we will have less depth of focus problem when defining very fine features.

4) Be precise with your technical language. Examples:
   (i) Grow an oxide is different from depositing an oxide;
   (ii) Either use diffusion or implantation, not to deposit a dopant;
   (iii) The n⁺ bottom plate of the capacitor is not a $V_T$ implant. It is heavily doped to act like a conductor.

**Problem 2**

(a) $(0.5 - x) \cdot 2.17 = 0.5 \Rightarrow x = 0.27 \mu m$

(b) (i) $R_p = 0.5 \mu m, \Delta R_p = 0.09 \mu m$

The boron will need a kinetic energy of 186 keV

(A) For $B^+$ ions, we need 186kV accelerating voltage

(B) For $BF_2^+$ ions, we need $186 \times \frac{11+19+19}{11} = 828$ kV accelerating voltage

(ii) $N_p = \frac{10^{13}}{\sqrt{2\pi\Delta R_p}} = 4.4 \times 10^{17}$/cm$^3$

$\therefore 4.4 \times 10^{17} e^{(x_j - R_p)^2/2\Delta R_p} = 10^{15}$

$\therefore (x_j - R_p)^2 = 2(0.09)^2 \cdot \ln\left(\frac{4.4 \times 10^{17}}{10^{15}}\right) = 0.099 \mu m^2$

$\therefore x_j = R_p \pm 0.314 \mu m$

For $x_1$: $x_1 = R_p - 0.314 = 0.186 \mu m$

(iii) $N_o = 4.4 \times 10^{17}$/cm$^3$, $N_B = 10^{15}$/cm$^3$, half-gaussian profile of p into n-type substrate.

The Irvin’s curves gives $R_S x_j = 2000$ ohm-$\mu m$.

Since $x_j = 0.314 \mu m$, therefore $R_S = 6400$ ohm/square
Problem 3

(a) We need **small** minimum resolution but **large** depth of focus for IC processing. The later is due to nonplanar surface topography of device structures. Since both min resolution and DOF is proportional to wavelength \( \lambda \), making \( \lambda \) smaller will not satisfy both requirements simultaneously.

(b) \[ R = r (\delta T_m \alpha_m - \delta T Si \alpha_Si) \]
The worst case for thermal run-out is illustrated in the attached figure with \( \delta T_m = 2^\circ C \) and \( \delta T Si = -2^\circ C \).

Lithography Step #1

\[ \begin{align*}
\text{mask} & \quad -1^\circ C \\
\text{wafer} & \quad +1^\circ C
\end{align*} \]

Lithography Step #2

\[ \begin{align*}
\text{mask} & \quad +1^\circ C \\
\text{wafer} & \quad -1^\circ C
\end{align*} \]

\[ \therefore R_{max} = 50 \text{mm} \times (1.6 \times 10^{-5} + 4.6 \times 10^{-6}) = 1.03 \mu m. \]

(c) (1) Light reflection from the slope can cause local increase of exposure which leads to linewidth variation during resist development. ARC reduces this reflection.
(2) Less reflected beam gives less standing wave effect, which gives also less variation of linewidth.
(3) Resist has more uniform thickness due to ARC layer planarization. The required development time can be more uniform. Less linewidth variation also.

(d) From the Grove model, we have: \( x_{ox}^2 + A x_{ox} = B(t+\tau) \)

Therefore,

\[ 2x_{ox} \frac{dx_{ox}}{dt} + A \frac{dx_{ox}}{dt} = B \]

or \( \frac{dx_{ox}}{dt} = \frac{B}{A + 2x_{ox}} \)

From \( 0.24 = \frac{B}{A + 0.5 \times 2} \) and \( 0.133 = \frac{B}{A + 1 \times 2} \), we get

\( A = 0.25 \mu m \) , \( B = 0.3 \mu m^2/\text{hour} \) and \( B/A = 1.2 \mu m/\text{hour} \)