# EE143 Fall 1992
Midterm #2
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Problem #1 (45 points) Diffusion

An emitter-base doping process is carried out on an arsenic doped substrate with 5x10^15 cm^-3 according to a four step process flow of:
1 Implant Boron 3x10^13 cm^-2
2 Drive 1075 C 60 min
3 Implant Phosphorus 1x10^15 cm^-2
4 Drive 1025 C 120 min

a) Find the depth of the junction formed by boron and arsenic.

b) Find the depth of the junction formed by phosphorus and boron.

c) Suppose an additional phenomena of field enhanced diffusion occurs with the following characteristics. It is only present at depths where one of the dopant concentrations exceeds n_i = 5x10^18 cm^-3. Here it produces an electric field which increases by 2 or more the diffusion coefficient of all species of the same type. This electric field also reduces the diffusion coefficient of all species of the opposite electrical type. Indicate on the sketch how the distributions of boron, phosphorus and arsenic change with this effect.
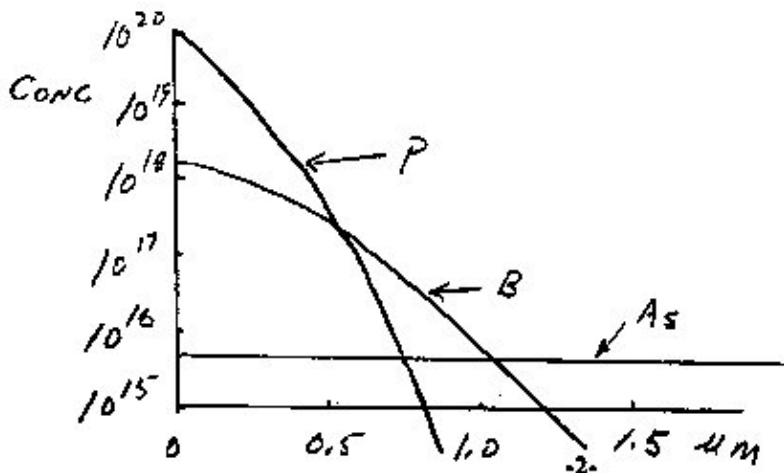
Problem #2 (30 points) Vacuum, Deposition and Etching

a) To what pressure should the chamber be pumped down to prevent the residual partial pressure of air from depositing 0.1% or less oxygen when aluminum is deposited at a rate of 0.2 um/min? Assume 21% of the partial pressure of air is due to O2.

b) On a single sketch show the difference in profile shape resulting from vertical and isotropic deposition of 1.0 um of material over the initial profile shown below. Give dimensions and descriptions of profile segments.
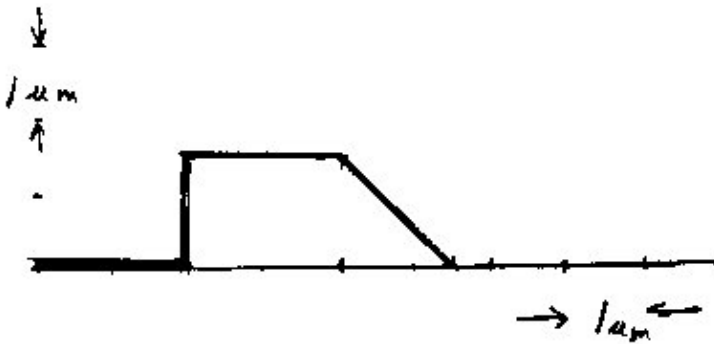
Problem #3 (30 points) Yield and Cost

a) A process consists of the sequential use of 5 modules. The chip area is 0.5 cm^2 and a 200mm wafer costs $1500 to process. Modules 1, 3 and 5 each have a defect density of 0.5 cm^-2. Modules 2 and 4 have yields of 0.80 and 0.70 respectively. What is the overall cost per good chip for the process?

b) Recommend a die area which will minimize the cost per working functionality. The cost is proportional to chip area. The yield is characterized by a defect density Do. The functionality is proportional to the chip area divided by the linewidth to the 2.5 power. The linewidth follows a trend of being inversely proportional to area.
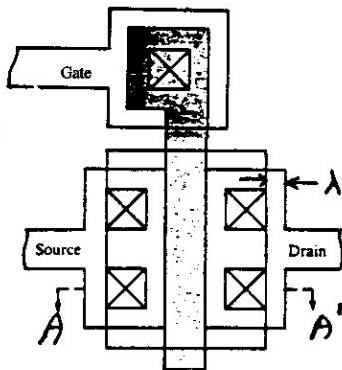
Problem #4 (40 points) Design Rules and Alignment

A 4 mask self-aligned NMOS process uses the layout and alignment sequence shown.
 Poly aligns to Active with error T1
 Contact aligns to Poly with error T2
 Metal aligns to Contact with error T3

The standard self-aligned process is given in Figure 1.5 pp. 8 of Jeager. Only go through the metal etch step.

a) Sketch the cross section of this device along the 'cut-line' AA' when misalignment has occured such that T1 is -1*lambda, T2 is zero and T3 is +1*lambda where all are measured along the horizontal direction in the layout.

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b) Describe at least 3 catastrophic failure mechanisms which can occur just as the misalignment errors exceed 1*lambda. Include a combination of T1, T2 and T3 in the horizontal or vertical direction in the layout at which the failure will take place.

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