Fall 2004

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE143 Midterm Exam #1

Family Name ______________________ First name __________________________

Signature ____

Make sure the exam paper has 6 pages (including cover page) + 2 pages of data for reference

Instructions: DO ALL WORK ON EXAM PAGES
This is a 90-minute exam (4 sheets of HANDWRITTEN notes allowed)

Grading:

- **To obtain full credit, show correct units and algebraic sign in answers. Numerical answers which are orders of magnitude off will receive no partial credit.**
- **For answers requiring explanations, adding sketches can be very effective.**

Problem 1 (30 points)________________

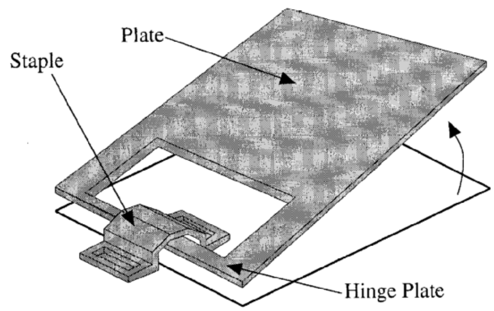
Problem 2 (30 points)_______________

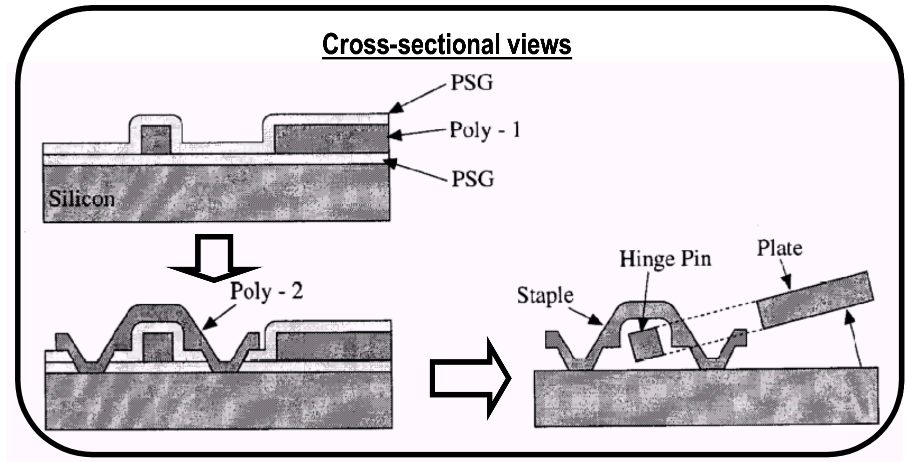
Problem 3 (40 points) ________________

TOTAL (100 points) __________________

Problem 1 Processing Steps and Simple Process Sequence (30 points total)

In class, we discussed a simple process flow to fabricate a hinge plate which can create an out-of-plane motion.





(i) (5 points) Starting with a blanket Si wafer, how many photolithography steps are used to fabricate this device. For each lithography step used, briefly describe its purpose.

(ii) (5 points) How many chemical vapor deposition (CVD) steps are used to fabricate this device. For each CVD step used, briefly describe its purpose.

(iii) (5 points) How many thin-film etching steps are used to fabricate this device. For each etching step used, briefly describe its purpose.

Problem 1 continued

(iv) (4 points) Can one form the staple structure **BEFORE** forming the hinge plate structure in the process sequence ? Explain why or why not .

(v) (4 points) Your lab partner suggests that poly-2 can be replaced by aluminum as the staple material. Do you agree or disagree with this suggestion? Justify your answer.

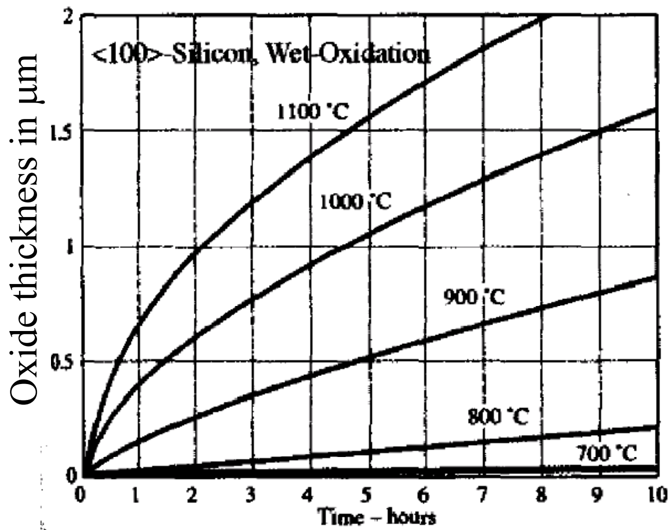
(vi) (7 points) Instead of using PSG as the sacrificial layer between poly-1 and poly-2, one can form a thermal oxide by oxidizing poly-1. **Sketch the cross-section of the final structure** after sacrificial layer removal. **Highlight/label the differences** between this cross-section and the one shown in the above figure.

Problem 2 Thermal oxidation (30 points total)

(a) You are given the following oxidation data for (100) Si : (1) B and B/A values for dry oxidation; and (2) the oxide thickness chart versus oxidation time for wet oxidation (initial oxide thickness = 0).

Rate constants for dry oxidation <100> Si

Oxidation Temp (^oC)	B (μm^2/hr)	B/A (μm/hr)
1200	0.045	0.667
1100	0.027	0.178
1000	0.0117	0.042



(i) (10 points) Starting with a blanket (100) Si wafer, how long does it take to grow a 0.2μm-thick SiO_2 with dry-oxygen at 1100^{o}C?

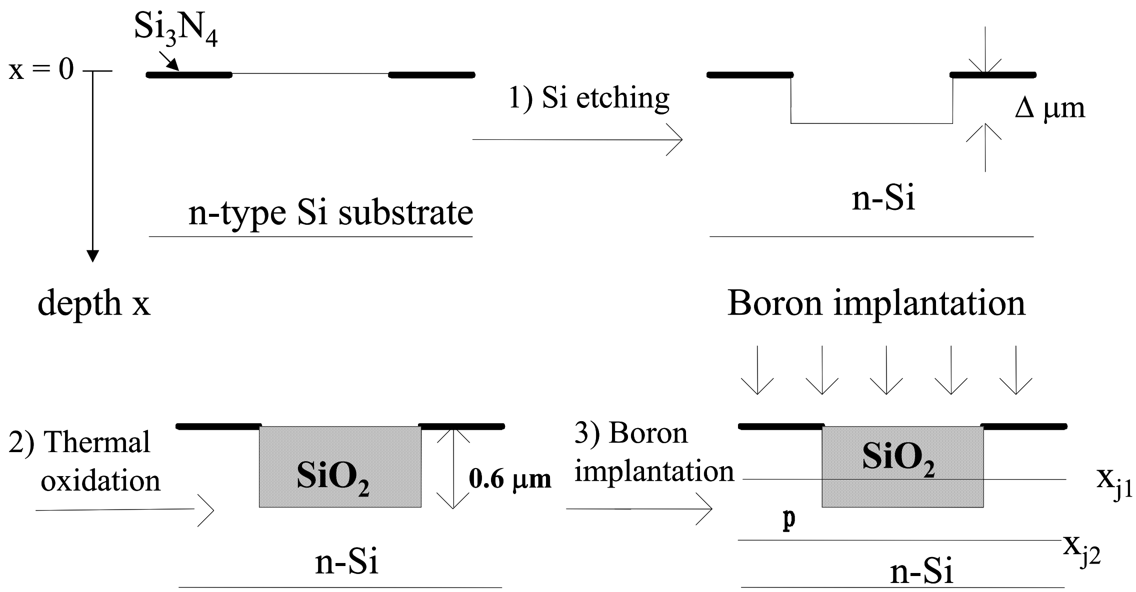
(ii) (10 points) The oxidized wafer in part (i) (with 0.2 μm oxide) is put back into furnace for wet oxidation at 1000^{o}C. How long will it take to grow an ***additional*** 0.3μm oxide ?

(b)(5 points) The Deal-Grove model for thermal oxidation will underestimate the oxide growth rate for thin oxides. How does one modify the model to describe the faster initial growth rate ?

(c) (5 points) By adding a few percent of HCl to oxygen will increase the oxidation rate. Explain.

Problem 3 Ion Implantation (40 points total)

The following schematic shows the process sequence to form a planarized SiO_2 trench by etching Si substrate, thermal oxidation, and followed by boron implantation.



(a) (5 points) For a SiO_2 trench thickness of 0.6 μm, calculate the required etched Si depth Δ .

(b) **Let us consider the region underneath the SiO2 trench**. We will assume the SiO_2 has identical ion stopping properties as Si , and the Si_3N_4 is infinitely thin. The boron (B^+) implantation (dose $=2 \times 10^{13}$ /cm^2) was performed such that only 50% of the implanted boron **dose** is incorporated inside the Si (the remaining dose is inside the SiO2).

(i) (5 points) Find out the required B^+ ion energy.

(ii)(10 points) The n-Si substrate has a background doping concentration $N_B = 1 \times 10^{15}$ /cm^3 .Calculate the junction depth x_{j2} (Surface of SiO2 is defined as x = 0)

Problem 3 continued

(iii) (10 points) Estimate the sheet resistance of the implanted boron layer at **regions underneath the SiO2 trench.** Show your calculations.

(c) (5 points) The boron implant profile in part (b) is assuming the ion beam is tilted slightly away from the <100> crystallographic axis of the Si wafer to avoid ion channeling. If the ion beam is exactly aligned with the <100> axis , compare the values of xj2 (deeper or shallower) for regions underneath the SiO2 trench and for regions underneath the Si3N4. Explain your reasoning.

(vi) (5 points) Quote an example and describe how the transverse straggle ΔR_t (also called lateral straggle) of implantation profile will affect the physical dimension of an integrated- circuit device.

Information which may be useful

1 μm = 10^{-4} cm = 1000nm = 10^{4} Å

Electron charge q= 1.6×10^{-19} coulombs;

Boltzmann constant k = 8.62×10^{-5} eV/K

n_i of Si = $3.69 \times 10^{16} \times T^{3/2} \exp[-0.605\text{eV}/kT]$ cm^{-3}

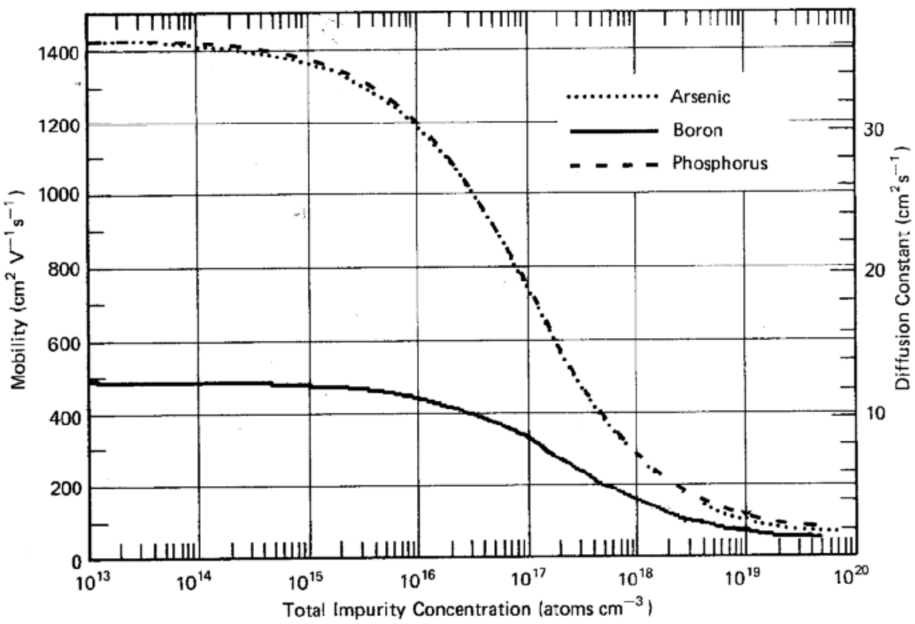
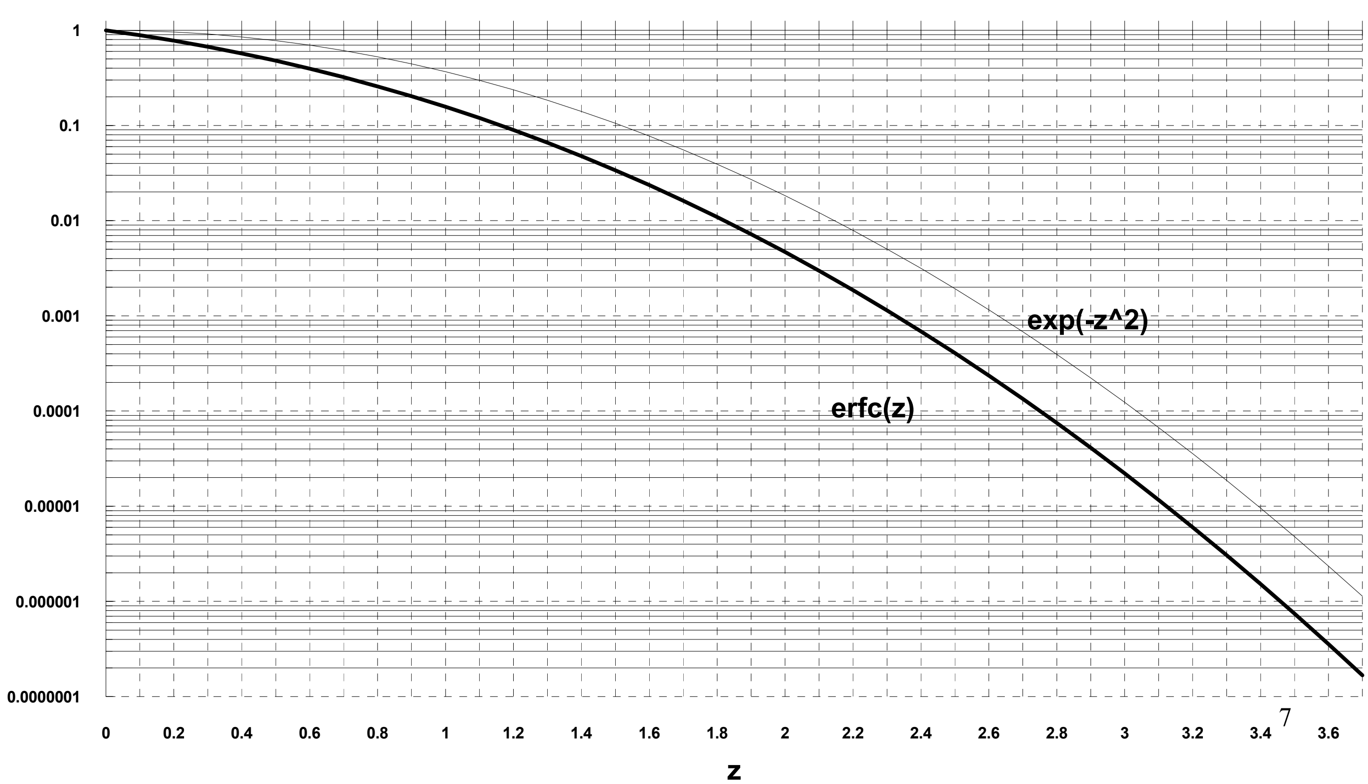
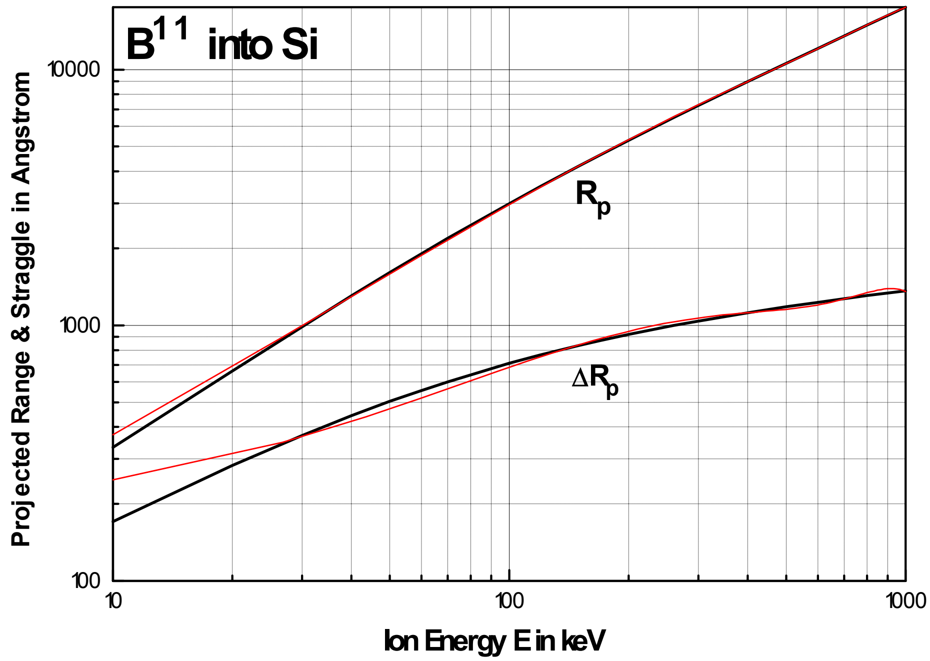


Figure 1.15 Electron and hole mobilities in silicon at 300 K as functions of the total dopant concentration. The values plotted are the results of curve fitting measurements from several sources. The mobility curves can be generated using Equation 1.2.10 with the following parameter values:[3]



$$R_p = 51.051 + 32.60883\,E - 0.03837\,E^2 + 3.758e{-5}\,E^3 - 1.433e{-8}\,E^4$$

$$\Delta R_p = 185.34201 + 6.5308\,E - 0.01745\,E^2 + 2.098e{-5}\,E^3 - 8.884e{-9}\,E^4$$



$$R_p = -7.14745 + 12.33417\,E + 0.00323\,E^2 - 8.086e{-6}\,E^3 + 3.766e{-9}\,E^4$$

$$\Delta R_p = 24.39576 + 4.93641\,E - 0.00697\,E^2 + 5.858e{-6}\,E^3 - 2.024e{-9}\,E^4$$