UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS143 Final Exam (Fall 2001)

Family Name_____ **First Name**_____

Signature_____

Instructions: DO ALL WORK ON EXAM PAGES

Make sure your copy of the exam paper has 13 pages (including cover page).
This is a 3-hr exam (12 sheets of notes allowed)

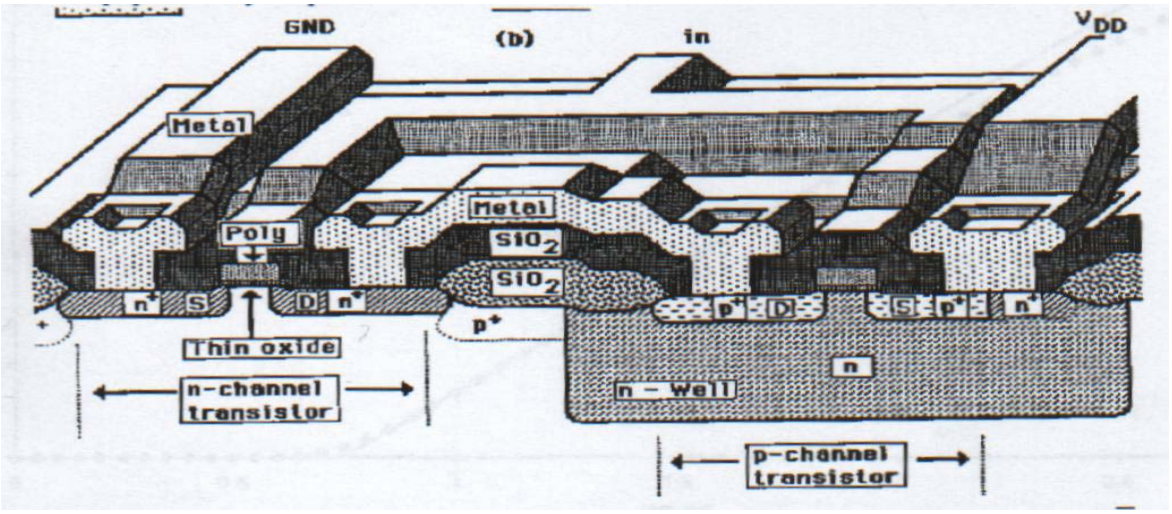
Grading: Whenever possible, use sketches to support your explanation. Show correct units and algebraic sign for numerical answers. No partial credit for numerical answers orders of magnitude off.

Problem 1 (25 points) _____	**Information which may be useful**
Problem 2 (20 points) _____	$\varepsilon_s := 1.036 \cdot 10^{-12} \cdot \frac{F}{cm}$ for Si $\varepsilon_{ox} := 3.45 \cdot 10^{-13} \cdot \frac{F}{cm}$ for SiO2
Problem 3 (25 points) _____	$q := 1.6 \cdot 10^{-19} \cdot coulombs$
	Boltzmann constant $k := 8.62 \cdot 10^{-5} \cdot \frac{eV}{k}$
	ni of Si $:= 1.45 \cdot 10^{10} \cdot cm^{-3}$ at 300K
Problem 4 (35 points) _____	Eg of Si $:= 1.12 \cdot eV$
	Electron Affinity of Si $:= 4.14 \cdot eV$
	Electric potential $\phi := (E_f - E_i)\, q$
Problem 5 (35 points) _____	$n := ni \cdot \exp\left(q \cdot \frac{\phi}{k \cdot T}\right)$ $X_d := \left[(2) \cdot \frac{\varepsilon_s}{q} \cdot (\phi_i - V_a) \cdot \left(\frac{1}{N_a} + \frac{1}{N_d}\right)\right]^{\frac{1}{2}}$
Problem 6 (35 points) _____	MOS: $V_{GB} := \phi_{MS} + V_{OX} + V_{Si}$
	$V_{FB} := \phi_{MS} - \frac{1}{C_{ox}} \left[Q_f + \int_0^{x_{ox}} x \cdot \frac{\rho_{ox}(x)}{x_{ox}} dx\right]$
TOTAL (175 points) _____	MOSFET I-V (n-channel):
	$I_{DS} := \mu_n \cdot \frac{W}{L} \cdot C_{ox} \cdot \left[(V_G - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2}\right]$ (below saturation)
	$I_{Dsat} := \mu_n \cdot \frac{W}{L} \cdot C_{ox} \cdot \left[\frac{(V_G - V_T)^2}{2}\right]$ (above saturation)

Problem 1 Lab Questions (25 points total)

(a) (15 points) In Cory 218, we only have the following processing equipment:
Quintel mask aligner
Photoresist spinning, baking, and development setups
Wet chemical bench for cleaning and wet etching
Oxidation furnace
Annealing furnace
Al evaporator.

Suppose one would like to upgrade the IC part of the EE143 chip to include a generic CMOS process. Indicate what additional equipment will be needed in Cory 218 to fabricate the CMOS inverter shown below which uses aluminum-2%Si-1%Cu as the metal interconnect. Also, describe/justify usage of the additional equipment in your process flow.

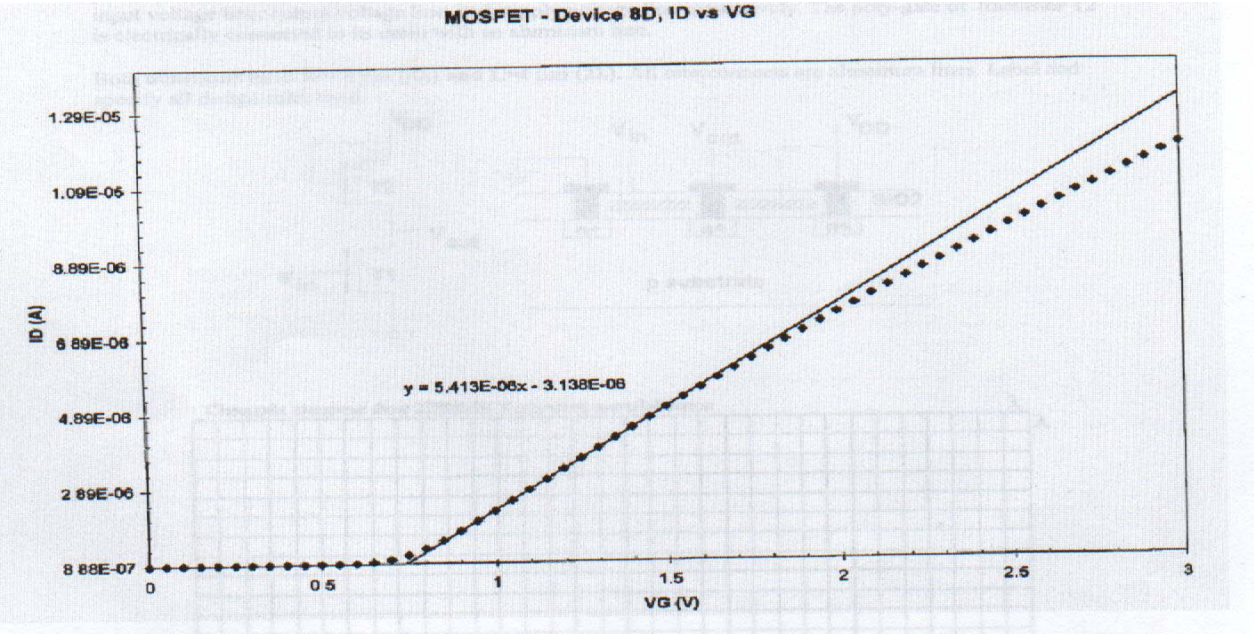


Additional Equipment	Describe/Justify usage in process steps

Problem 1 Lab questions continued

(b) The Id versus Vg plot of the EE143 MOSFET [Device 8D with W/L = 15um/10um] is shown below. The Vds bias is kept constant at 50mV.

MOSFET – Device 8D, Id vs Vg



y=5.413E-06x – 3.138E-08

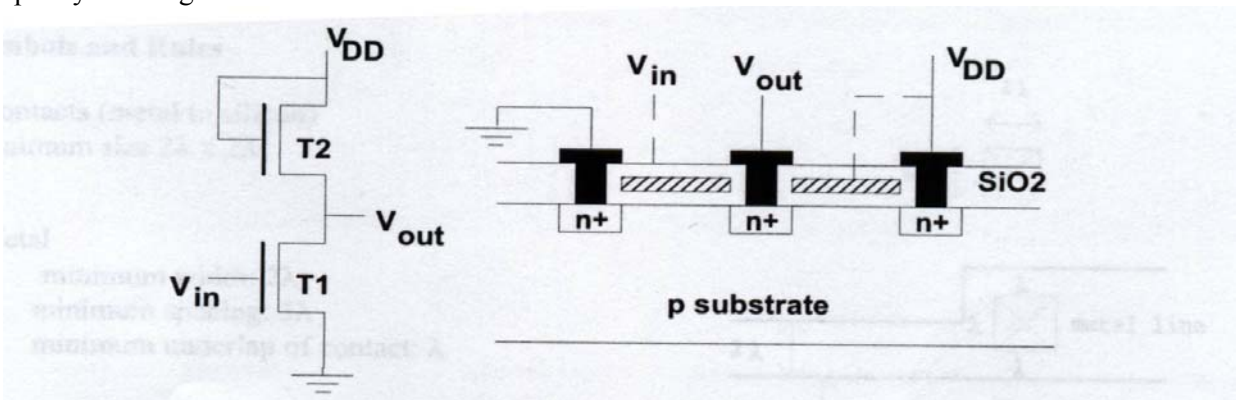
(i) (5 points) Extract the threshold voltage from the data. Show all your calculations.

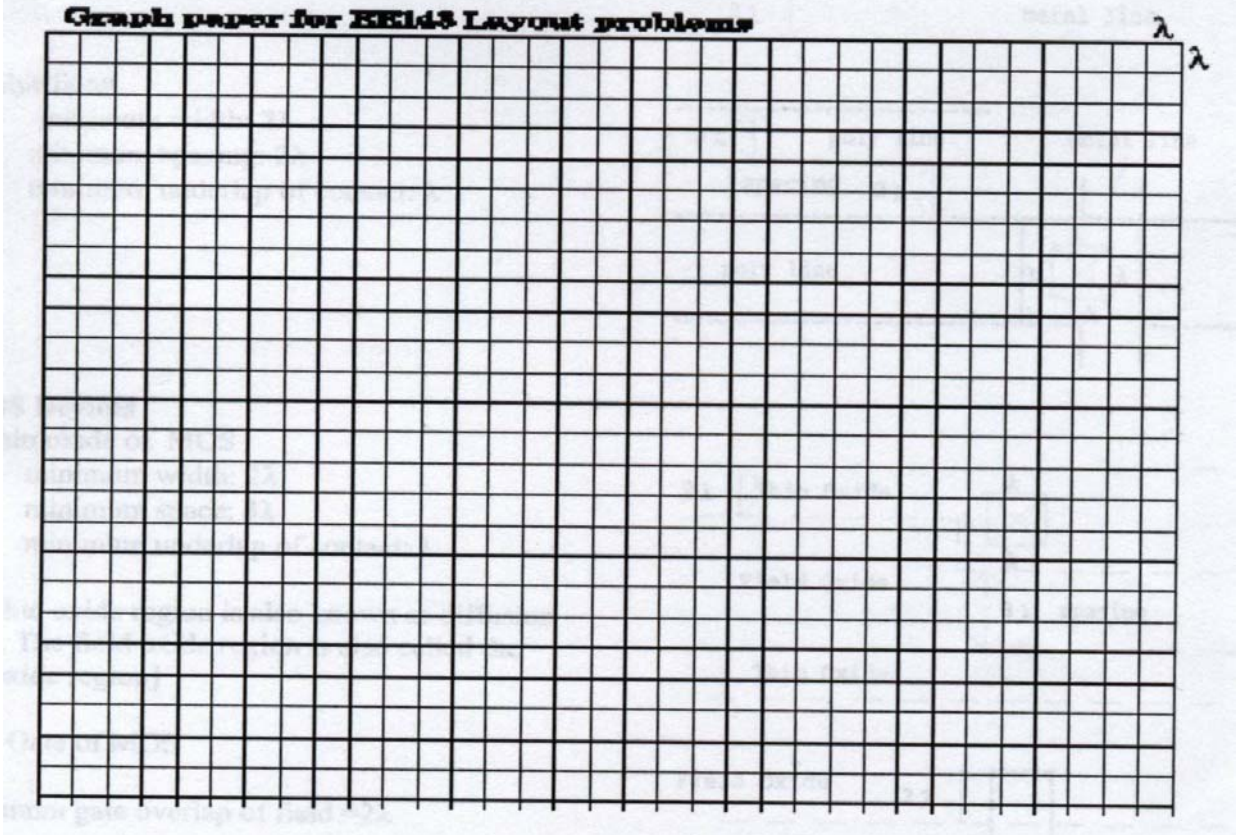
(ii) (5 points) From C-V measurement, we know the gate oxide thickness 73nm. Extract the channel electron mobility μn from the I_V data. Show all your calculations.

Problem 2 Layout (20 points total)

Layout a minimum geometry NMOS (poly-gate) inverter with the EE143 design rules in the graph paper provided. The circuit diagram and the schematic cross-section are shown below. Vin, Vout and Vdd are the input voltage line, output voltage line, and supply voltage line respectively. The poly-gate of transistor T2 is electrically connected to its drain with an aluminum line.

Both transistors have W= 8μm (4λ) and L= 4μm (2λ). All interconnects are aluminum lines. Label and specify all design rules used.





Reference: EE143 Standard Layout symbols and Design Rules

1. Background

1.1 Lithography/etching limit on minimum feature or spacing = 2λ
1.2 Alignment limit (overlay accuracy) = λ
1.3 Unless specified, default value: λ = 2μm

2. Symbols and Rules

2.1 Contacts (metal to silicon)
minimum size 2λ x 2λ

2.2 Metal
minimum width: 2λ
minimum spacing: 3λ
minimum underlap of contact: λ

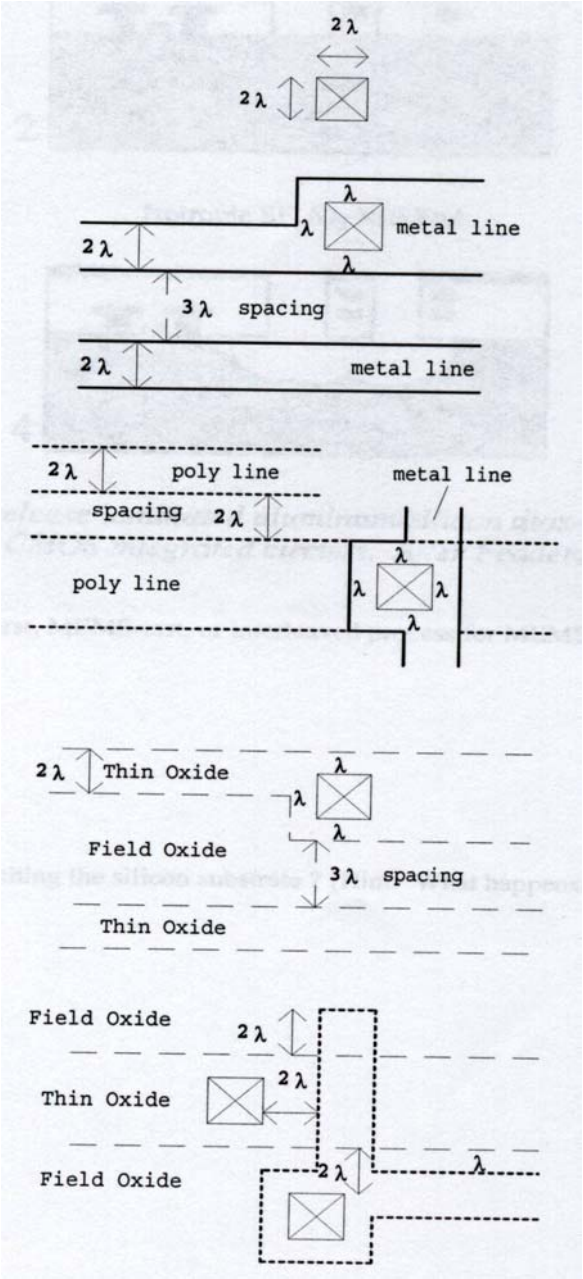
2.3 Polysilicon
minimum width: 2λ
minimum spacing: 2λ
minimum underlap of contact: λ

3. MOS Devices

3.1 Thin oxide of MOS
minimum width: 2λ
minimum spacing: 3λ
minimum underlap of contact: λ

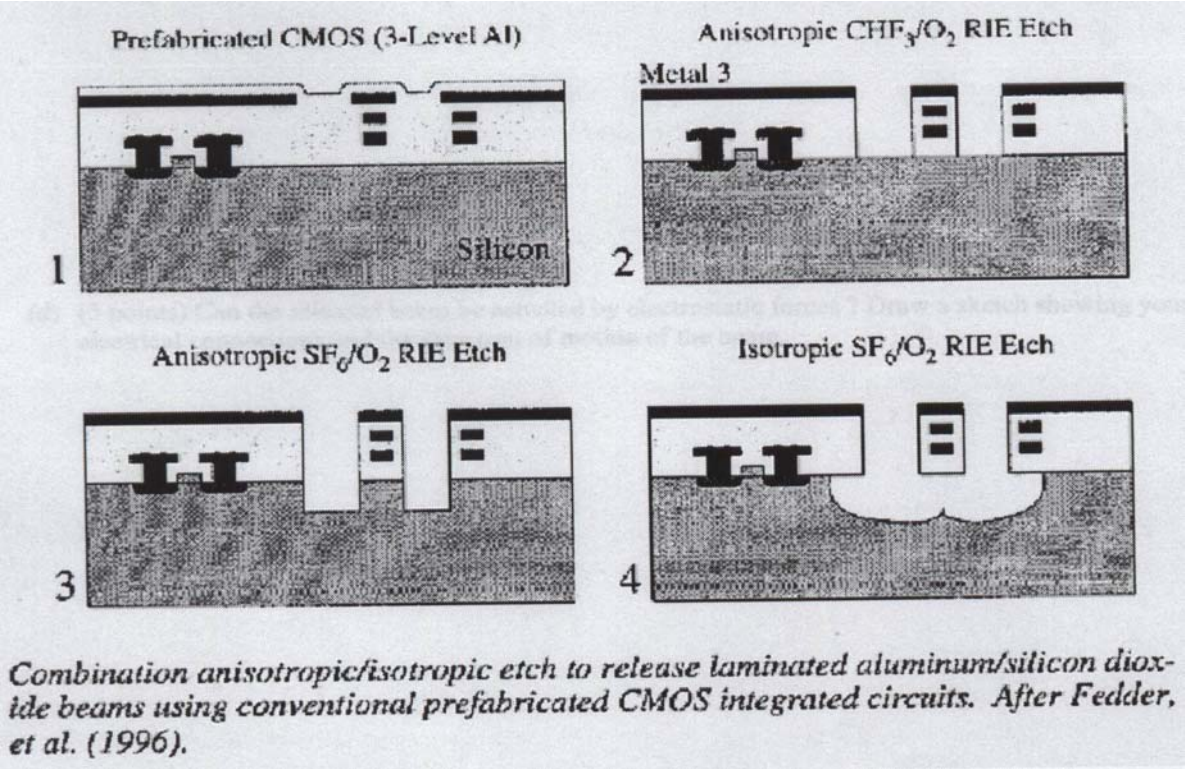
[The thin oxide region is also known as diffusion region. The field oxide region is also called the thick oxide region]

3.2 Si Gate of MOS
Minimum gate overlap of field = 2λ
Minimum contact to gate spacing = 2λ
Contacts to polysilicon allowed on thick oxide only. Minimum spacing to thin oxide =2λ
Minimum poly to think oxide spacing = λ



Problem 3 MEMS Fabrication (25 points total)

The following schematic shows the sequence of integrating CMOS with laminated oxide/aluminum cantilever beam structures.



Combination anisotropic/isotropic etch to release laminated aluminum/silicon dioxide beams using conventional prefabricated CMOS integrated circuits. After Fedder, et al. (1996).

a) (5 points) Will you consider this as a MEMS-first, MEMS-last, or interleaved process for MEMS-IC Integration? Briefly explain.

b) (5 points) For Step 3, what is the purpose of etching the silicon substrate? [Hint: What happens if one skips Step 3?]

Problem 3 continued

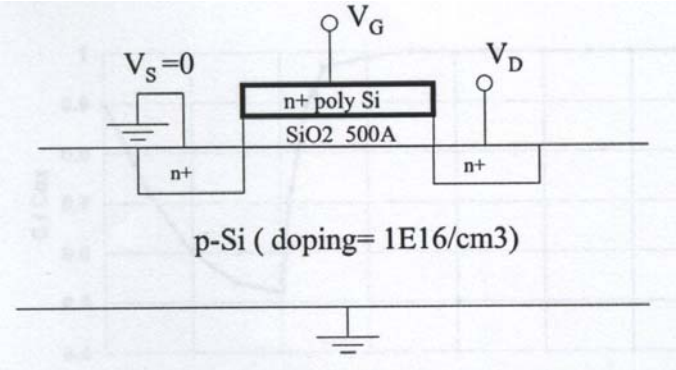
c) (5 points) For Step 4, what advantage is to release the beam by a RIE process instead of using a wet etch for the silicon substrate?

d) (5 points) Can the released beam be actuated by electrostatic forces? Draw a sketch showing your electrical connections and the direction of motion of the beam.

e) (5 points) List a couple of limitations of this process from the MEMS perspective.

Problem 4 MOS Calculations (35 points total)

The following cross-section shows a NMOS transistor with n+ poly_Si gate, gate oxide thickness = 500 A, and a p-substrate with doping concentration = 1E16/cm^3.



a)

(i) (9points) If there is no oxide or oxide interface, calculate the threshold voltage Vt for Vd = 0.

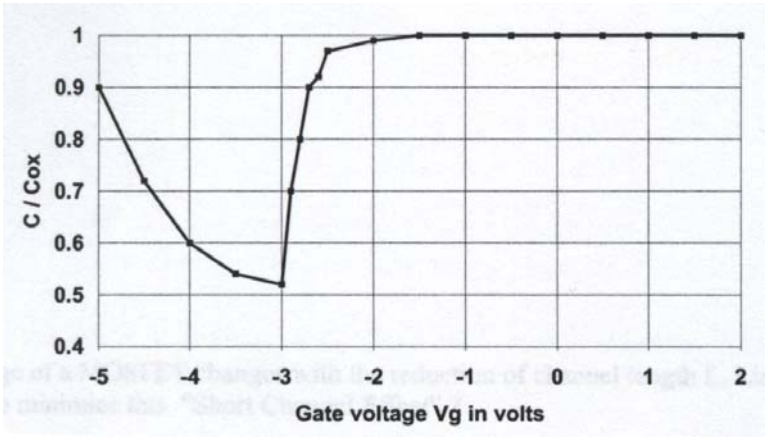
(ii) (3 points) Calculate the drain current for Vg = Vd = 3V. Use k = uA/V^2.
Note: Ids (triode region) = k[(Vg=Vt)Vds-Vds^2/2]; Ids (saturation region) = k[(Vg-Vt)^2/2]

(iii) (3 points) After exposing the MOSFET to cosmic radiation which creates an oxide interface charge Qf, the threshold voltage shifts upward by +8 volts [i.e., ΔVt = +8 volts]. Determine the sign and magnitude of Qf.

(iv) (3 points) What is the drain current for Vg = Vd = 3 volts after the MOSFET is exposed to cosmic radiation?

Problem 4 continued

b) (5 points) Experimentall data of C/Cox versus Vg are given below for a MOS capacitor. It is known that the oxide thickness is 0.26μm. Calculate the maximum depletion layer thickness, Xdmax.



c) (15 points) Indicate in the table below how the parameters of a n-channel MOSFET will change when the (i) gate work function Φm, (ii) substrate doping concentration Na, or (iii) gate oxide thickness Xox increases. Indicate increase, decrease, or no change.

	Vt	Xdmax	Vdsat	Idsat	gmsat
Φm(increases)					
Na(increases)					
Xox(increases)					

Problem 5 General Questions (35 points total, 5 points each)

a) Discuss why n+ ultra-shallow junctions (Xj < 0.1μm) are easier to fabricate than p+ ultra-shallow junctions.

b) Threshold voltage of a MOSFET changes with the reduction of channel length L. List two processing approaches taken to minimize this "Short Channel Effect"?

c) List some advantages and disadvantages of using larger diameter Si wafers (e.g 300mm diameter) for IC processing.

d) Minimum feature printing by optical lithography is proportional to λ/NA. However, if λ is extremely small (e.g wavelength of hard X-ray), minimum resolution degrades. What is the physical mechanism which degrades the resolution?

Problem 5 continued

e) Sketch the cross-section of a SALICIDE structure and list two advantages of the SALICIDE process.

f) Why do we need low dielectric material as insulator in multilayer metallization? Also, name two potential candidates as low-K material.

g) For MEMS processing, residual stress and stress gradients of thin films can create curved cantilever structures or buckled membranes. What are the general approaches to minimize the curvature and buckling?

Problem 6 Process Integration Questions (35 points total, 5 points each)

The following process integration description on shallow trench isolation (STI) is taken from a textbook Read the description and answer the questions on the next page.

Deep trench isolation is extremely difficult to manufacture and it is difficult to integrate with random logic when arbitrary device spacings must be accommodated. The development of chemical mechanical polishing (CMP) has made previously rejected shallow trench isolation (STI) a viable process since it can remove the excess deposited oxide without a lithography step. As shown in Figure 15.13, the process begins with a pad oxide of 100 to 150 Å, followed by a layer 1500 to 2000 Å of LPCVD Si_3N_4. Next a field is patterned and the nitride, oxide, and silicon are etched. Typical etch depths are about 0.5 μm thick. Trench sidewalls are etched at 75 to 80°. If desired, a field implant can then be done now to prevent inversion under the trench, or it can be delayed until after the polishing step is sufficiently high energy is used. Next a thin (150 to 200 Å) layer of SiO_2 is grown thermally to reduce the etch damage on the sidewalls and round off some of the corners. A 0.9- to 1.1-μm layer of SiO_2 is then deposited, usually by high-density PECVD, and CMP is used to remove the excess oxide. The nitride serves as a polish stop for this step. Finally the nitride is removed and the pad oxide stripped in HF [22].

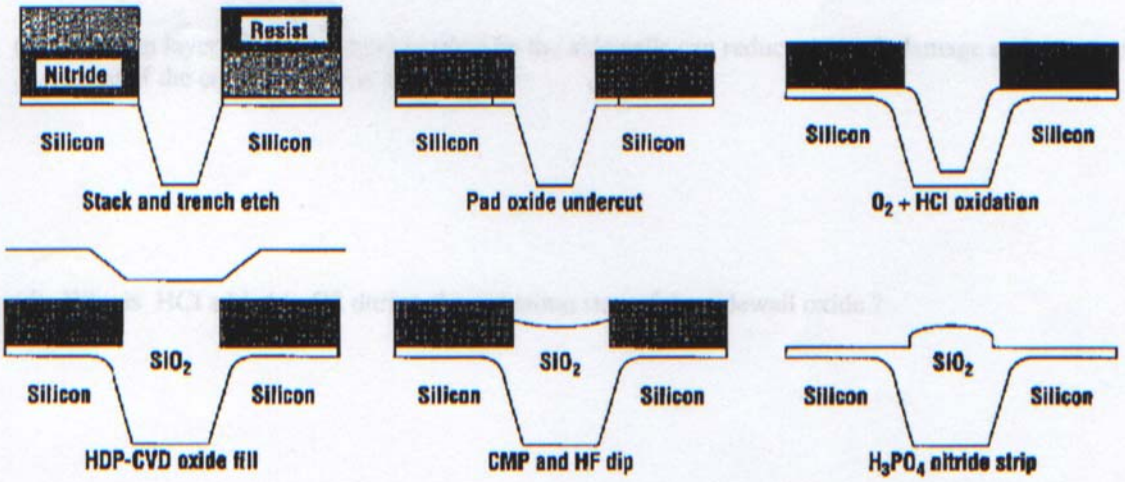


Figure 15.13 Schematic of a shallow trench isolation module *(after Chaterjee et al., used with permission, APS, 1997).*

The integration of STI presents a number of challenging problems. Some of these problems are associated with the upper corner. Typically in an MOS transistor, the gate polysilicon stripe extends onto the field oxide to ensure a separation between the source and drain. If the corner of the STI is too sharp, the trench sidewall will invert (due to field concentration) leading to excess subthreshold leakage. This is especially a problem if the CMP is overdone, that it, if the top of the planarized oxide is below the top of the silicon [23]. To avoid this problem the trench walls must be properly tapered and the top corner must be rounded. To achieve the desired rounding, the pad oxide is selectively removed by undercutting the nitride layer, then oxidized using high oxidation temperatures (~1100°C) and/or an ambient containing HCl. CMP dishing leads to a thinning of the field oxide [24] and may lead to a design rule for the maximum isolation distance and/or the use of dummy active areas [25].

Problem 6 continued

a) Describe why deep trench isolation is extremely difficult when arbitrary device spaings must be accommodated. Use sketches to illustrate if necessary.

b) Compare the two cross-sections after sidewall oxidation with (i) pad oxide undercut, and (ii) without pad oxide undercut. Point out the difference.

c) The thin layer of thermal oxide grown on the sidewalls can reduce the etch damage and round off some of the corners. Why is that?

d) Why is HCl added to O2 during the oxidation step of the sidewall oxide?

e) If the field implant is delayed until after the polishing step, describe how it will be done. Use sketches to illustrate if necessary.

f) What is the advantage to use high-density PECVD to deposit the refill oxide?

g) If there is CMP dishing, sketch the cross-section of a finished transistor and indicate which part of the sidewall is more likely to invert.