I. Static Analysis

1a) (20 pts) Set up an equation for $V_{out}$ and solve for $V_{out}$ to an accuracy of 0.2 volts when $V_a = 3V$ and $V_b = 5V$.

![Circuit Diagram]

1b) (20 pts) Find the minimum value of $(W/L)p$ such that when $V_a = 5V$ and $V_b = 0V$, the output voltage (including the 100 $\mu$A current) will be less than or equal to 1.5V. Note that both $V_a$ and $V_b$ have changed from part a.

II. Transient Analysis of CMOS
Rpmos = 30 kohms / (W/L)p
Rnmos = 10 kohms / (W/L)n
For each source or drain
Cdbp = 1.0 fF x (W/L)p
Cdbn = 1.5 fF x (W/L)n

2a) (15 pts) Assuming the only capacitance present is Cl, find the worst case propagation delay.

2b) (15 pts) Using the Cdbp and Cdbn values given above and the (W/L) sizes shown, find the total internal capacitance which has the possibility of changing voltage.

2c) (10 pts) Find the worst case propagation delay when both Cl and the Cdb internal capacitances are present.

III. CCMOS and Standard Cells
3a) (15 pts) Sketch the circuit and find the logic function of the standard cells STICK Diagram.

3b) (15 pts) Design a standard cells STICKS diagram for \( F(\overline{b}) = \overline{a}bc + de + f \)

IV. Pass Transistor and Body Effect

4a) (15 pts) Find the logic function generated by the circuit below and explain how \( F \) is well defined for all possible 8 input combinations.
4b) (15 pts) List 5 reasons why \( t_{phl} \) and \( t_{plh} \) can be unequal.