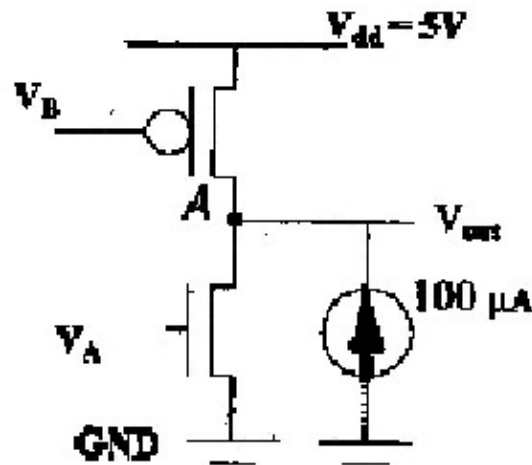


**EECS 141, Spring 1999
Midterm 1
Professor Neureuther**

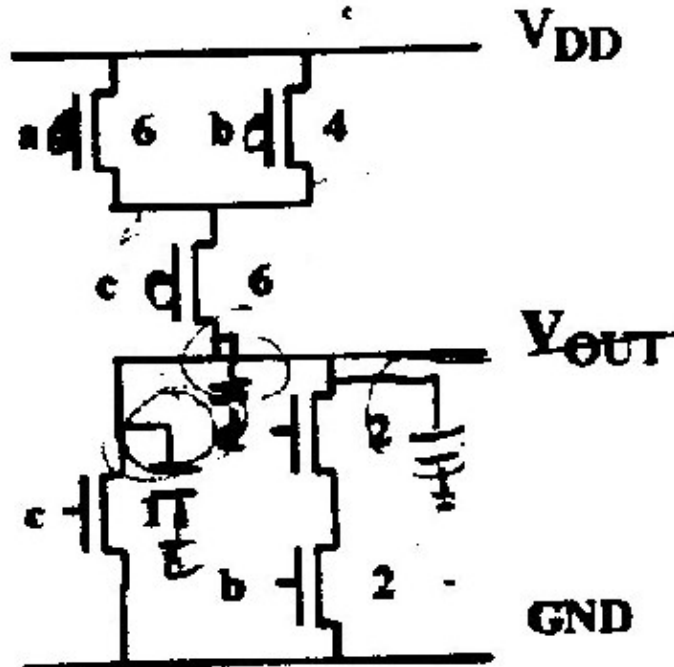
I. Static Analysis

1a) (20 pts) Set up an equation for V_{out} and solve for V_{out} to an accuracy of 0.2 volts when $V_a = 3V$ and $V_b = 5V$.



1b) (20 pts) Find the minimum value of $(W/L)_p$ such that when $V_a = 5V$ and $V_b = 0V$, the output voltage (including the $100 \mu A$ current) will be less than or equal to $1.5V$. Note that both V_a and V_b have changed from part a.

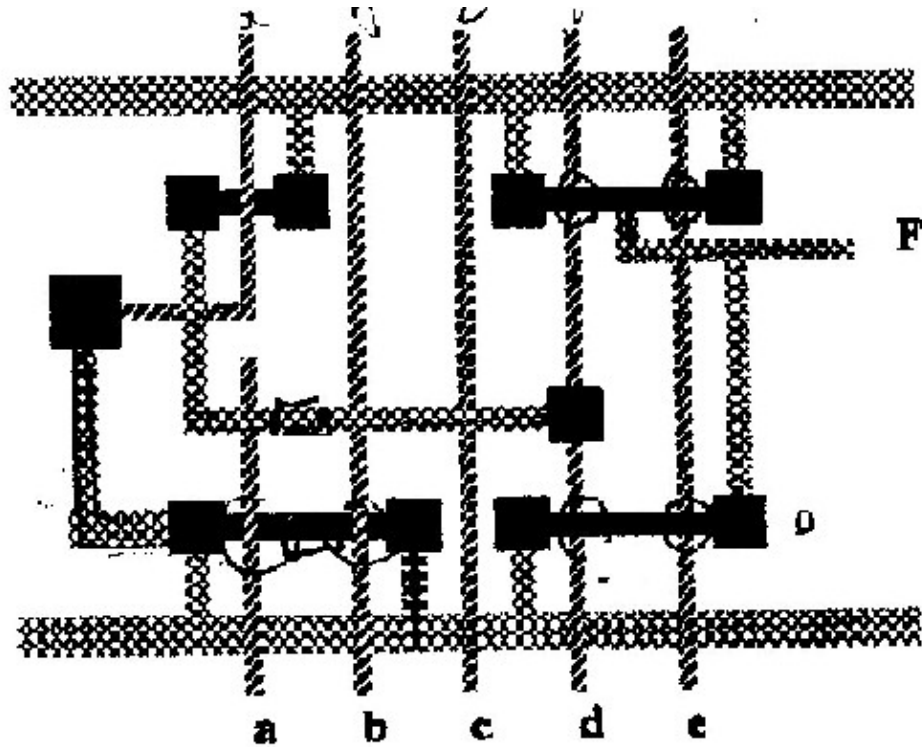
II. Transient Analysis of CMOS



$R_{pmos} = 30 \text{ kohms} / (W/L)_p$
 $R_{nmos} = 10 \text{ kohms} / (W/L)_n$
 For each source or drain
 $C_{dbp} = 1.0 \text{ fF} \times (W/L)_p$
 $C_{dbn} = 1.5 \text{ fF} \times (W/L)_n$

- 2a)** (15 pts) Assuming the only capacitance present is C_l , find the worst case propagation delay.
2b) (15 pts) Using the C_{dbp} and C_{dbn} values given above and the (W/L) sizes shown, find the total internal capacitance which has the possibility of changing voltage.
2c) (10 pts) Find the worst case propagation delay when both C_l and the C_{db} internal capacitances are present.

III. CCMOS and Standard Cells

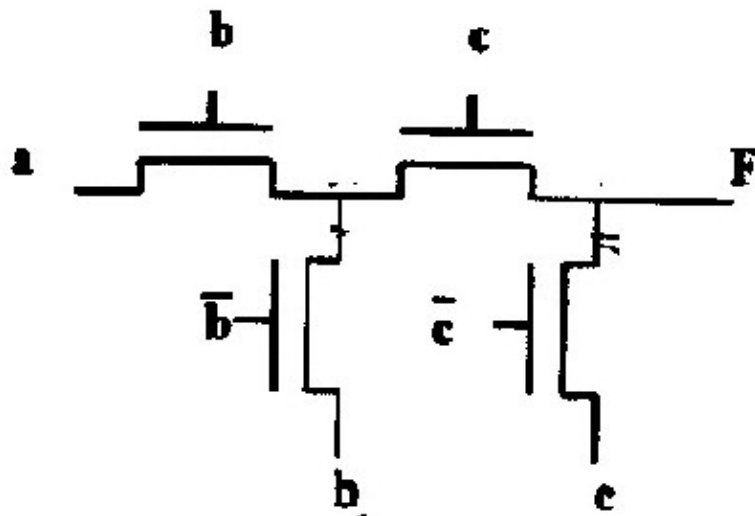


3a) (15 pts) Sketch the circuit and find the logic function of the standard cells STICK Diagram.

3b) (15 pts) Design a standard cells STICKS diagram for $F(\text{bar}) = abc + de + f$

IV. Pass Transistor and Body Effect

4a) (15 pts) Find the logic function generated by the circuit below and explain how F is well defined for all possible 8 input combinations.



4b) (15 pts) List 5 reasons why t_{pHL} and t_{pLH} can be unequal.

Posted by HKN (Electrical Engineering and Computer Science Honor Society)

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