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EECS 141: SPRING 98 —MIDTERM 2

For all problems, you can assume the following transistor parameters:

NMOS:

$V_{Tn} = 0.75V$, $k'_n = 20\ \mu A/V^2$, $\lambda = 0$, $\gamma = 0.5\ V^{1/2}$, $2\Phi_F = -0.6V$

PMOS:

$V_{Tp} = -0.75V$, $k'_p = 7\ \mu A/V^2$, $\lambda = 0$, $\gamma = 0.5\ V^{1/2}$, $2\Phi_F = -0.6V$

NAME	Last First

GRAD/UNDERGRAD	

Problem 1:

Problem 2:

Problem 3:

Total	

Problem 1: Arithmetic

Jane Doe, a UC Berkeley EECS 141 is requested to design a logarithmic shifter based on pass-transistor logic that takes as input a 16-bit word and supports a programmable shift to the right (i.e. downwards) between 0 and 15 bit.

a. Assume that the shifter network is implemented using minimum-size transistors with the following parameters: R_{eq} = 10 kΩ, C_{db} = C_{sb} = 10 fF, C_{gb} = 15 fF (all other capacitances may be ignored). The capacitance at the output node equals 50 fF. **Draw the resistor-capacitor network that represents to the worst-case delay of the network**, and annotate the meaningful component values. Give a first-order approximation of the delay of the network. No buffering should be included at this point.

tp =

b. Jane has heard (on the grapevine) that the worst-case delay of the network can be reduced by introducing buffers in the network. She decides to introduce two buffers. Her library supports a buffer with a delay of 400 psec (independent of the load - waw!) and an input capacitance and output capacitance of 20 fF. Draw a diagram indicating where she should introduce the buffers. Derive an expression for the worst-case delay of the network and determine its value.

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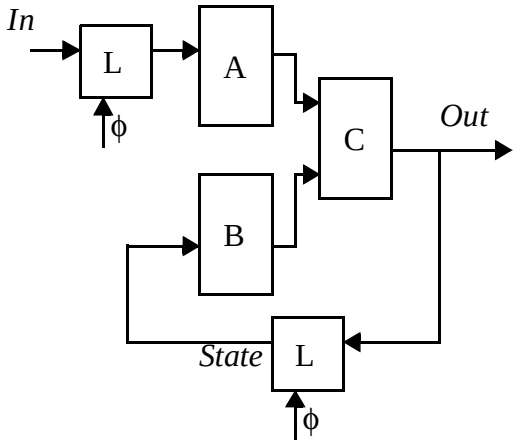
PROBLEM 2: Sequential Circuits

a. Consider the simple logic network shown below. A, B, and C represent combinational logic blocks with the following properties:



t_{minA} = 200 psec; t_{maxA} = 1 nsec;
t_{minB} = 300 psec; t_{maxB} = 2 nsec;
t_{minC} = 100 psec; t_{maxC} = 0.5 nsec;

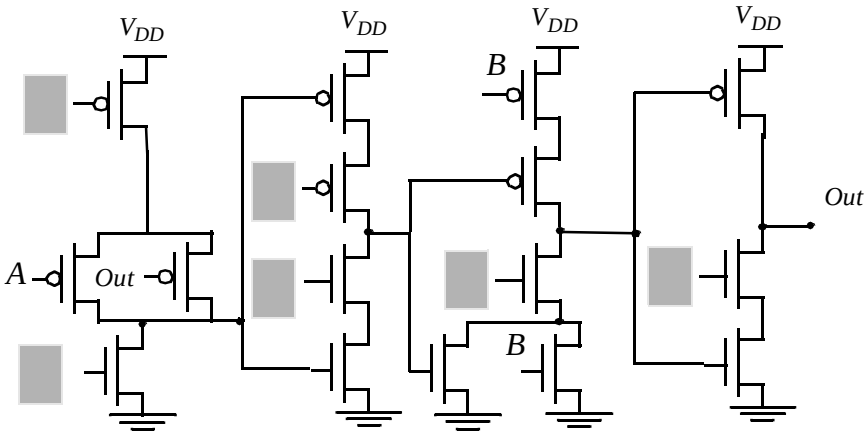
The L-units represent **latches** clocked by ϕ. L has a setup time of 150 psec and a delay of 250 psec. The clock ϕ has a period T and is high for a duration of T_{on}. The duty cycle of the clock hence equals 100 T_{on}/T %.

a. Determine the conditions on the clock necessary to avoid the occurrence of races.

b. Determine the absolute minimum clock period for this circuit to work correctly. State your assumptions on the clock duty cycle.

PROBLEM 3: Sequential Circuits

Consider the sequential circuit shown below.



a. Fill in the missing clock connections on the schematics (marked by the gray boxes) so that the circuit will operate correctly. For each connection you can choose between ϕ and $\overline{\phi}$ (you may assume here that they are non-overlapping and that there is no skew).

b. For each gate in the circuit, fill in the operation mode of the gate for the given clock mode in the table below (choose between **precharge**, **eval**, and **hold**).

	Gate 1	Gate 2	Gate 3	Gate 4
ϕ				
$\overline{\phi}$				

c. The above circuit has some room for simplification. Describe in a couple of sentences how you would simplify the circuit (and the resulting benefit) without sacrificing functional correctness.

PROBLEM 4: Logic styles and power

A designer has to implement a 6-input AND gate. He has available a library containing the cell-types enumerated below together with their properties in terms of capacitance.

	Inv	NOR2	NOR3	NAND2	NAND3	NAND6
Cin	48 fF	48 fF	48 fF	48 fF	48 fF	48 fF
Cout	85 fF	101 fF	117 fF	105 fF	132 fF	200 fF

a. Determine the average power dissipation of an implementation using a 6-input NAND (and an inverter). The circuit operates at a supply voltage of 3V and a clock frequency of 20 MHz. Assume that all the inputs have an equal chance of being 0 or 1. You may ignore the power dissipated by the 6 input signals.

Pav =

b. Implement the same function using predominantly 3-input NANDs (plus some others gates). Draw the schematic of the circuit you will be using and determine the power dissipation.

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c. Assume now that the design of part b. is laid out with dynamic gates instead. Assume that this reduces all the capacitances with a factor of 2. All gates however have an additional clock input with a capacitance equal to 20 fF. Determine the power here as well..

d. Consider the following questions:

d.1 Under what conditions can the circuit of part b) display **dynamic hazards**?

d.2 Same question for the circuit of part c).