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EECS 141: SPRING 98 — FINAL

For all problems, you can assume the following transistor parameters:

NMOS:

V_{Tn} = 0.75V, k'_n = 20 μA/V^2, λ = 0, γ = 0.5 $V^{1/2}$, $2\Phi_F$ = -0.6V, LD = 0.15 μm

PMOS:

V_{Tp} = -0.75V, k'_p = 7 μA/V^2, λ = 0, γ = 0.5 $V^{1/2}$, $2\Phi_F$ = -0.6V, LD = 0.15 μm

NAME	Last First

GRAD/UNDERGRAD	

Problem 1:
Problem 2:
Problem 3:
Problem 4:
Problem 5:
Problem 6:

Total	

Have a wonderful summer!

Problem 1: Multivibrators

a. Shown in Figure 1 is a novel design of a Schmitt trigger. Determine the (W/L) ratio of transistor M1 so that $V_{M+} = 3\ V_{Tn}$. VDD = 3.3V. You may ignore the body effect in this question. State clearly your other assumptions.

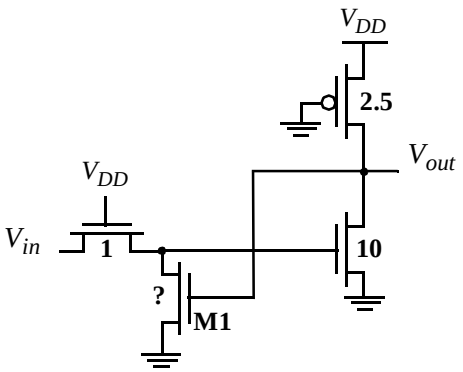


FIG. 1 Schmitt trigger. Numbers on transistors indicate (W/L) ratio's.

$(W/L)_{M1}$=

b. Determine approximately the value of V_{M-}.

V_{M-}=

c. Figure 2 shows a monostable multivibrator. Draw the waveforms for nodes V_{in}, X, Y, and V_{out} and annotate the appropriate voltage values. VDD = 3.3 V.

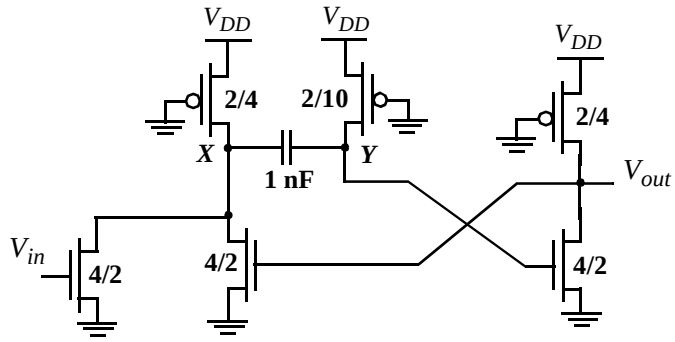


FIG. 2 Monostable multivibrator

d. Calculate the output pulse width.

T_{width} =

Problem 2. Logic

Consider the logic family shown in Figure 3.

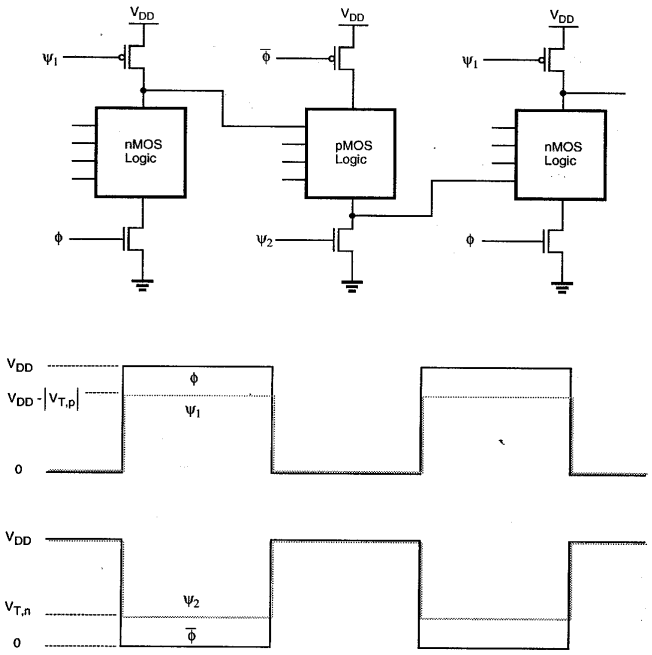


FIG. 3 Novel logic family

a. Explain in a couple of sentences the advantage of using the clocking strategy shown in Figure 3.

advantage 1.

advantage 2.

advantage 3.

b. Mark the characteristics that are valid for this logic family.

o Clock-feedthrough helps to improve the performance

o Cascading gates can lead to problems

o The preferred logic gate from a power perspective is the NAND gate

o Cooling the circuit helps to reduce the minimum clock frequency.

c. Two chips operating at different voltages have to be connected together. The straightforward approach would be to just connect the output and input gates, as shown in Figure 4. Mention 3 major problems of this approach.

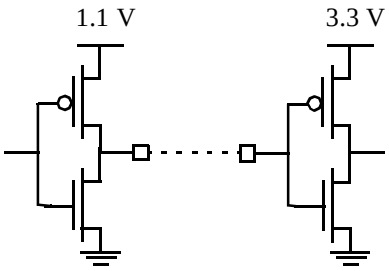


FIG. 4 Interconnecting chips operating at different voltages

problem 1.

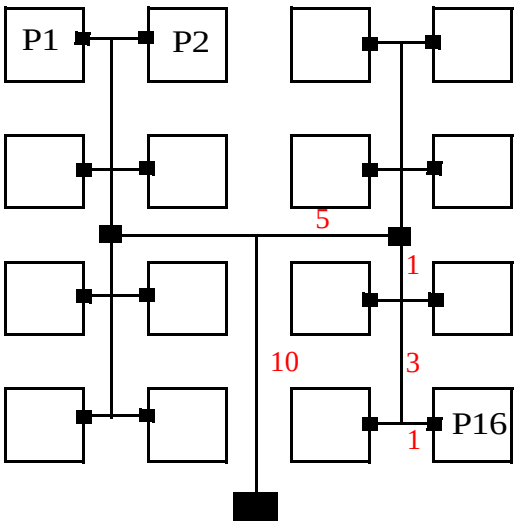
problem 2.

problem 3.

d. Propose TWO simple modifications in the circuit to deal with most of the mentioned problems. **YOU MAY AT MOST ADD ONE TRANSISTOR.**

Problem 3: Timing

In order to boost profits, Intel has decided that their next-generation microprocessor has to have ultimate performance. To achive the desired performance, 16 processors are integrated on the same die (the chip is hence called the *seidecium* - for obvious reasons). The designer of the clocking architecture has come up with the strategy shown in the Figure below. A single clock-signal is distributed over the complete chip. Three levels of buffering are used as shown by the black boxes in the Figure.



Important parameters:

r_{wire} = 0.3 kΩ/cm

c_{wire} = 0.25 pF/cm

t_{buffer} (level 1,2, and 3) = 0.5 nsec

FIG. 5 Seidecium Processor clock distribution network. The numbers annotated on the figure indicate the lengths of the wiring segments (in cm)

a. Determine the maximum skew between the different processor modules.

$skew_{max}$ =

b. The goal of the designers is to reach of a 500 MHz clock speed. Determine the maximum delay of the logical function blocks given that only 75% of the clock period can typically used for computation (due to set-up and hold times of the registers). Also, note that the maximum internal skew within a processor module equals 150 psec.

t_{plogic} =

c. The Intel designers forgot to account for one thing though. Due to the parameters variations over the die, it is observed that the delay of the clock buffers can vary over 25% (in both positive and negative directions). Determine the worst-case clock speed due to these variations.

f_{max} =

Problem 4: Memory

Consider the memory architecture shown in the Figure below.

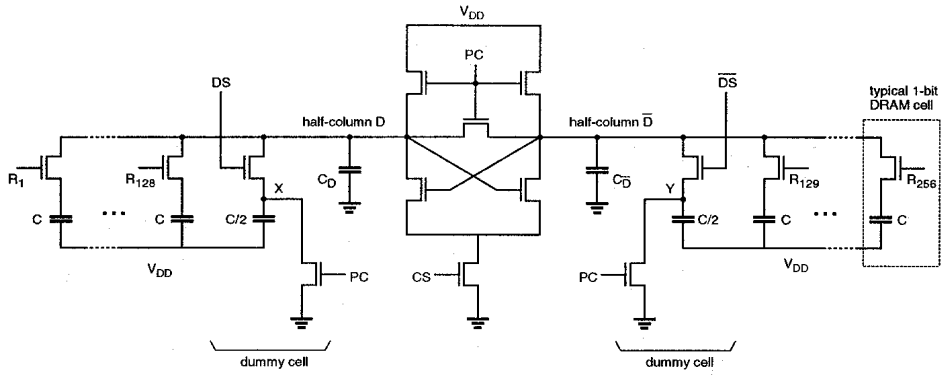
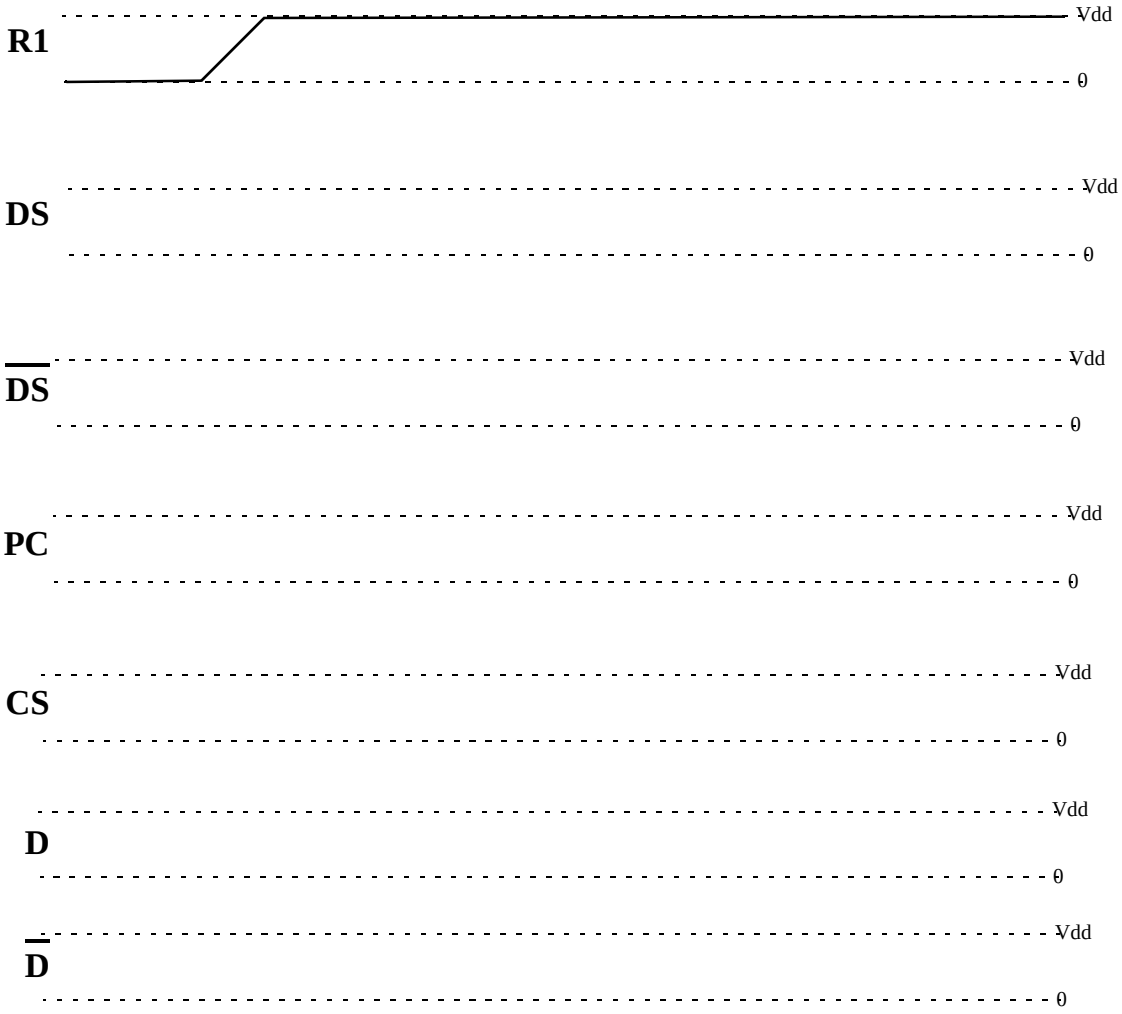


FIG. 6 Memory architecture

a. Draw the (approximated) waveforms for the signals mentioned.



b. Assuming the following memory parameters C_D = 500 fF, determine the minimum value of C_S so that the voltage difference on the bit lines during a read operation equals at least 200 mV. V_{DD} = 2.5V. You may ignore body-effect for this problem.

C_S =

c. Disaster can strike any second. A passing alpha particle may reduce the charge stored in a cell with 30 fC. Determine how you would adjust the cell capacitor value so that a 200 mV read signal is still guaranteed on the bitlines even after an alpha particle has struck.

C_S =

d. Explain why boosting the wordline voltages above V_{DD} helps to improve the performance.

Problem 5: Interconnect

An ee141 student (unnamed) figures out (s)he can get a successful multi-million $ start-up going by designing receivers (RX) for systems as defined below. Assume that the transmission line is implemented on a PCB with $\nu = 13$ cm/nsec. Assume also CMOS full-wing levels for the TX input.

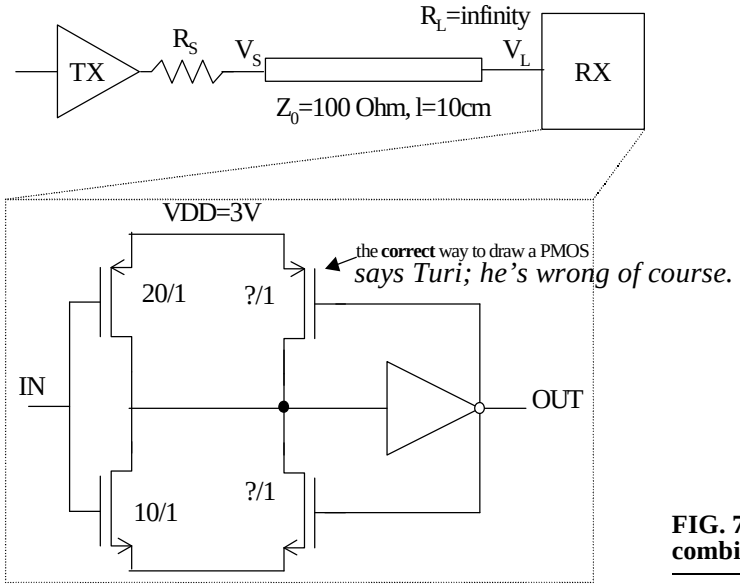


FIG. 7 Transmitter-Receiver combination

a. Unfortunately, the designer of the TX does not understand transmission lines and sets R_s to 10 Ω. Draw the lattice diagram that includes the first three values of V_L.

b. Using your answer in part a, or a stated assumption regarding the waveform at V_L, derive the transistor sizing for the receiver (shown in the figure above) that prevents glitching after an initial signal transition , but requires the smallest input swing (hint: pick the smallest transistors that still avoid glitches).

c. After raising hell with the TX designer, R_s is raised to 500 Ω, and our ee141 graduate replaces the receiver drawn with a conventional inverter. What is the shortest clock period that allows V_L to reach 50% of its final value? (assume $V_M = V_{DD}/2$ and that the TX input switches instantaneously).

T_{min} =

Problem 6. Interconnect

a. Derive a global expression of the **typical gate (being an inverter) delay** in the presence of wiring with a length equal to L_{net} followed by a fanout of 4 equivalent gates. Make sure to include all components. You may assume that the following parameters are given: C_{gate}, R_{on} (of driver), R_{int} (per unit length), and C_{int} (per unit length). You may assume that the diffusion capacitance at the output of the gate is approximately equal to its gate capacitance. **Clearly state all other assumptions you are making**.

b. Discuss how you would reduce the delay if the capacitive load of the fanout is the dominant factor and discuss the optimium value.

c. Discuss how you would reduce the delay if the interconnect delay is the dominant factor.

d. Derive an expression for the minimum delay in the latter case.