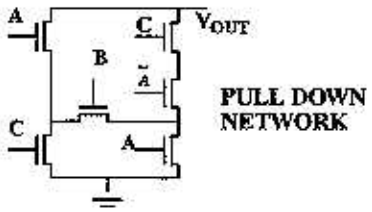
EE141: Spring 1995 - Final Exam

Wednesday, May 17, 1995 Open Book, Open Notes, Wirte directly on this exam.

CMOS Parameters:
This exam is to be worked using the stand device models in the Rabaey for MOS(pp.50, 53, 66) and Bipolar(pp. 77, 83) devices unless otherwise specified in the problem.

I. (45 Points) Complementary CMOS



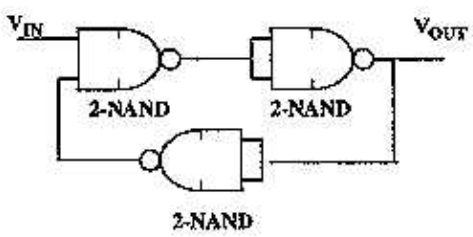
I.a.(20 Points) Pull Up Network

Draw the Pull Up Network to complete the complementary CMOS gate and give an Euler path if one exists.

I.b.(25 Points) Sticks Digram of Layout

Create a Sticks Diagram using a **continuous diffusion** if possible. You may use more than one poly for each input and you may assume that both the input and its complement are available. Be sure to label all poly, diffusion, ground, Vout.

II.IIa(70 Points) Sequential Circuits and Logic Styles



Operation
At t =0 V_{IN} goes from 0 to 1 and then remains at 1.

RC Model for Parts b), c) and d)
All minimum sized devices
$R_{NMOS} = 10\ k\Omega$, $R_{PMOS} = 30\ k\Omega$
$C_{GATE} = 4\ fF$
$C_{SOURCE} = C_{DRAIN} = 5\ fF$

II.a.(15 Points) Overall Circuit Function

Describe the output as a function of time based on less of loading have a delay of 0.5ns. Specify any delay, pulse widths, pulse sequences, etc.

II.b.(20 Points) Redesign

Assuming the 2-input NAND gates are Complementary CMOS with minimum sized devices. Use an RC switch level model to estimate the delay from the input at t = 0 to the 50% transition of the output.

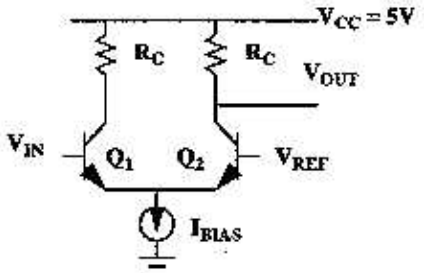
II.c(15 Points) Use of Extra Inputs

Specify a fixed voltage for the duplicate inputs for the second and third NAND gates such that the circuit will still function. Then use the RC switch level model to estimate the delay from the input to the 50% transition of the output.

II.d.(20 Points) Pseudo NMOS

The initial circuit is now to be implemented in psuedo-NMOS. Use the RC switch level model to estimate the delay from the input to the 50% transition of the output. Assume the pseudo-NMOS load has a W/L = 1/4 with **Ron = 4 Rpmos, Cgate = 16 fF and Cdrain = Csource = 5 fF**.

III.(50 Points) Bipolar



$V_{REF} = 4.2V$
$\beta = 100$
$V_{BE(on)} = 0.7$ V
$V_{CE(SAT)} = 0.1$ V
$\tau_{LIFE} = 1$ ns
Ignore all junction capacitance

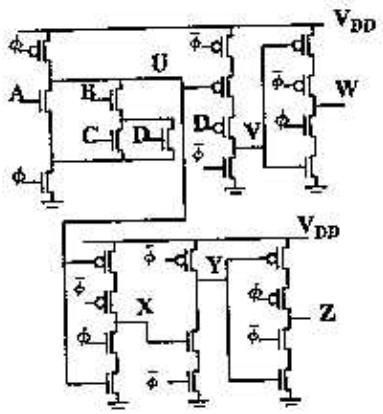
III.a(20 Points) ECL Static Analysis

Design the bias current Ibias and load resister Rc such that the power consumption is 1 mW and transistor Q1 saturates at Vin = 0.45V.

III.b.(30 Points) Transient

Find the minority charge in the base of Q1 when Vin is 4.2 V and all the current flows through Q1. Determine how long it takes for Vout of another gate to remove the minority charge. You may simplify the problem by assuming that Vin remains at 4.2 V.

(65 Points) Dynamic Logic and latches



Conditions

A = 1, B = 1, C = 0, D = 0
ϕ low for long time
W = 1, X = 1

Model

All minimum sized devices
R_{NMOS} = 10 kΩ, R_{PMOS} = 30 kΩ
C_{GATE} = 4 fF
$C_{SOURCE} = C_{DRAIN}$ = 5 fF

IV.a.(15 Points) Intital Values

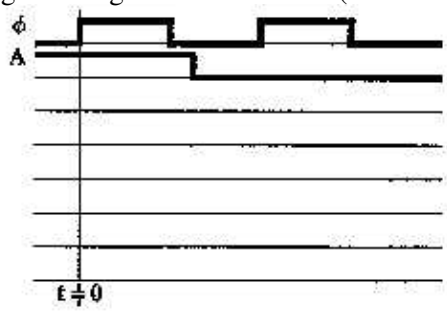
Determine the intial value of U, V, Y, and Z.

IV.b.(20 Points) Propagation Delay

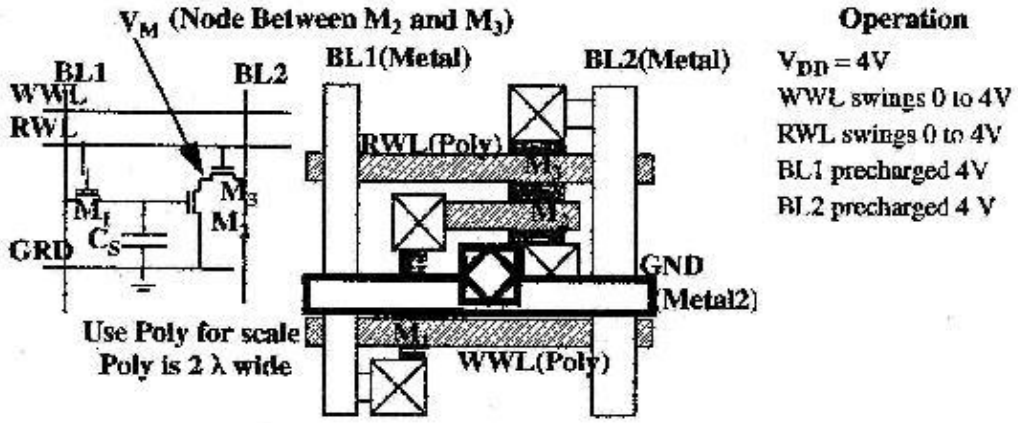
Use the RC switch level model to determine the propagation delay from the rising edge of the clock to the 50% transition of V.

IV.c.(30 Points) Dynamic Operation

Neglecting rise and fall times, find W and Z as a function of time for two clock cycles. Note that input **A** changes during this time as well. (show results for intermediate signals for partial credit.)



V.(70 Points) Memory



V.a.(15 Points) Circuit Drive and Bit Line Change

Assuming minimum sized devices and Vm = 2V, find the slew rate(volts/second) for **BL2** if it has a capacitance of 2 pF. Neglect Body Effect.

V.b.(25 Points) Sizing and Body Effect

Size M2 such that Vm will be 2V. Besure to include the **BODY EFFECT** on all devices.

V.c(15 Points) RC Delay and Layout

If the maximum read word line (RWL) delay is to be 1ns, find how many DRAM Cells could be placed in series. (Model poly as being either over field or gate and neglect inter conductor capacitances.)

V.d.(15 Points) Charge Sharing and Layout

If the read word line poly is floating during the charging of **BL2** from 0 to 4V by another circuit, what will be the voltage due to charge sharing on the read bit line? (Consider various sources of mutual capacitance.)