



University of California  
College of Engineering  
Department of Electrical Engineering  
and Computer Sciences

B. Nikolić

Tuesday, March 7, 2006  
6:40-8:00pm

## EECS 141: SPRING 2006 – MIDTERM 1

<b>NAME</b>	Last	First
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<b>GRAD/UNDERGRAD</b>	
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Problem 1: \_\_\_\_/14

Problem 2: \_\_\_\_/28

Problem 3: \_\_\_\_/16

Total: \_\_\_\_/58

**PROBLEM 1. (14 pts) CMOS logic gates.**

- a) (6pts) Implement the logic function  $Y = \overline{AB + (CD + E)}$  in a single CMOS logic gate.

- b) (8 pts) Draw a stick diagram for the logic gate from part a), with a goal to minimize the diffusion capacitance. Please use vertical lines for poly gates and horizontal lines for diffusion strips. Label your transistors.

**PROBLEM 2. (28 pts) Inverter and wiring delay.**

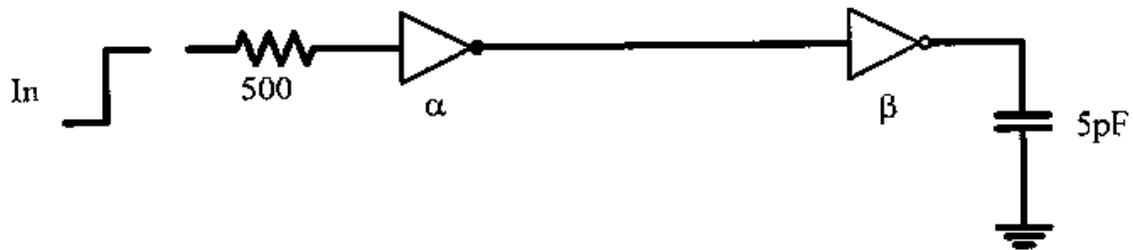


Figure 1

Figure 1 shows a pair of symmetrically sized inverters driving a large off-chip load. The first inverter is made of thin oxide transistors and has an intrinsic delay of 15ps. The second inverter is made with thick-oxide transistors for compatibility with higher voltages and has an intrinsic delay of 45ps. Assume that a symmetrical, unit-sized inverter has input capacitance  $C_g=2\text{fF}$  and  $\gamma=1$ , for both thick and thin oxide devices. The first inverter is driven by a logic gate that has an output resistance of  $500\Omega$ .

- a) (2pts) Find  $C_{\text{int}}$  and  $R_{\text{eq}}$  for a unit inverter made of standard transistors, and for a unit inverter made of thick-oxide transistors.

- b) (4 pts) Assume the size of the output inverter is given as  $\beta$ . Find the size of the first inverter,  $\alpha$ , in terms of  $\beta$ , that minimizes the overall delay.

c) (4 pts) Assume the size of the first inverter is given as  $\alpha$ . Find the size of the output inverter,  $\beta$ , in terms of  $\alpha$  that minimizes the overall delay.

d) (6 pts) From your answers for part b) and c) (or by any other way), solve for  $\alpha$  and  $\beta$ .

- e) (4 pts) The output inverter is at the edge of the chip near a bonding pad, while the first inverter is near the core of the chip. The inverters are connected by a metal-1 wire, 1mm long and 1 $\mu$ m wide. Assume the wire is over field oxide with no other wiring nearby. The sheet resistance of aluminum in metal layers 1 is 80m $\Omega$ / $\square$ . Fringing capacitance from metal-1 to substrate is 40aF/ $\mu$ m, and bottom-plate capacitance is 30aF/ $\mu$ m<sup>2</sup>. Find the equivalent lump-element resistance and capacitance for this wire. Sketch a schematic for a lumped RC model of the connection between the two inverters, including relevant capacitances and resistances from the inverters themselves.

- f) (8 pts) Assume the size of the output inverter is given as  $\beta$ . Find the size of the first inverter,  $\alpha$ , in terms of  $\beta$ , that minimizes the overall delay with wiring parasitics present.

**PROBLEM 3. (16 pts) Scaling.**

- a) (4pts) A company has implemented a single-core microprocessor in 90nm technology with 300mV threshold voltages, that operates at 3.8GHz with a 1.4V supply, with a 100W power dissipation, and a die size of  $200\text{mm}^2$ . They would like to build a dual core microprocessor in the same technology, by duplicating the single core design. At which frequency and supply voltage should the dual core design be running to maintain the same size of the heat sink? You can assume that the frequency of operation is roughly linearly proportional to the supply voltage in this technology.
- b) (6pts) If the single-core design is ported to a 65nm technology with a 1.2V supply, what would be its size, frequency of operation and power? You can assume that all of the power is switching power.



c) (2pts) According to the scaling rules, what should be the threshold voltage in the 1.2V 65nm technology, if the 90nm from part a) is the starting technology?

d) (4pts) If in a single-core design from part a), the total power of 100W was actually composed of 80% switching and 20% leakage, what would be the total power of a scaled processor in 65nm technology? Assume the subthreshold slope  $S = 80\text{mV/dec}$ .