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EECS 141: FALL 99 —MIDTERM 2

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):

NMOS:

$V_{Tn} = 0.4$, $k'_n = 115\ \mu A/V^2$, $V_{DSAT} = 0.6V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2\Phi_F = -0.6V$

PMOS:

$V_{Tp} = -0.4V$, $k'_p = -30\ \mu A/V^2$, $V_{DSAT} = -1V$, $\lambda = 0$, $\gamma = -0.4\ V^{1/2}$, $2\Phi_F = 0.6V$

NAME	Last SOLUTIONS First

GRAD/UNDERGRAD	

Problem 1: 5

Problem 2: 4

Problem 3: 4

Problem 4: 7

GOOD LUCK!!

Total	20

1. Pass-transistor Logic

A pass-transistor network is shown in FIG. 1. Assume that inputs A and B are ideal voltage sources. V_{DD} = 2.5V. The gate capacitances are constant and equal to 4fF, and all drain/source capacitances are equal to 2fF (all these capacitances can be considered as capacitances to ground). The load capacitor connected to the output is C_L =10 fF. The equivalent resistance of an NMOS transistor with W/L=1 is 15kΩ, while the equivalent resistance of a PMOS with W/L = 1 equals 50kΩ. The NMOS transistors have W/L=2 and PMOS transistors have W/L=4.

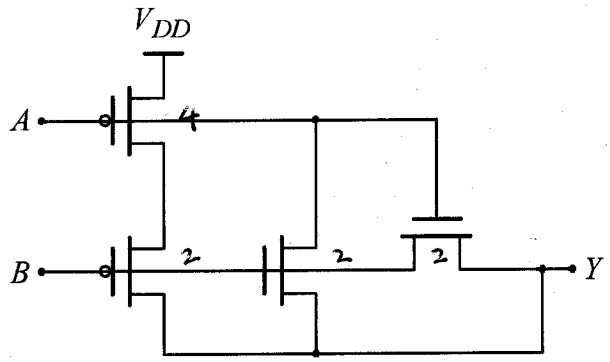

FIG. 1 Pass-transistor network

a. For all the possible combinations of inputs A and B find the output voltage levels.

A	*B*	*Y*
0	0	$V_{DD} = 2.5V$
0	V_{DD}	ϕ
V_{DD}	0	ϕ
V_{DD}	V_{DD}	$V_{DD} - V_T = 1.86V$

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_f - V_{SB}|} - \sqrt{|2\phi_f|}\right)$$
$$= 0.4 + 0.4\left[\sqrt{2.5 - 0.6} - \sqrt{0.6}\right]$$
$$= 0.64V$$

b) What logic function $Y = f(A, B)$ is implemented by this network?

$Y = \overline{A \oplus B} = A$ XNOR B

c) Find the propagation delay (from $V_{DD}/2$ to $V_{DD}/2$) of this network when $B = 0$, and A switches instantaneously from V_{DD} to 0.

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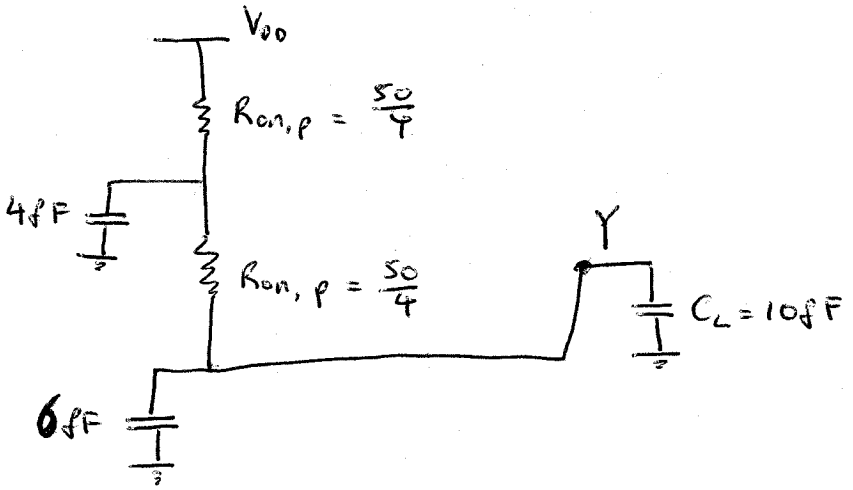
From $V_{DD}/2$ to $V_{DD}/2$ simply means the propagation delay as we have defined in class from 2nd week.



$$\tau = 4f\left(\frac{50k}{4}\right) + 16f\left(\frac{100k}{4}\right) = 450ps$$

$$t_p = 0.69\,\tau = 310ps$$

2. Miscellaneous Problems

a. The complementary CMOS circuit shown in the Figure is used in the more complex network shown below. Indicate **2 ways** on how you would modify the CMOS circuit such that the delay between Z_0 and F_{out} is minimized (you are to stick to static complementary static CMOS). Redraw the circuit if needed.

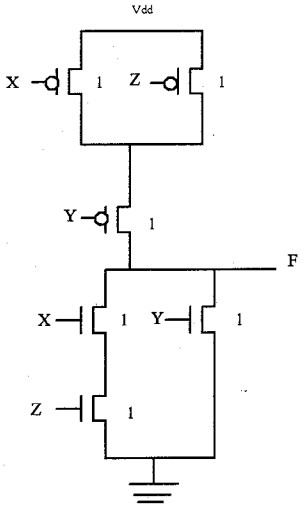
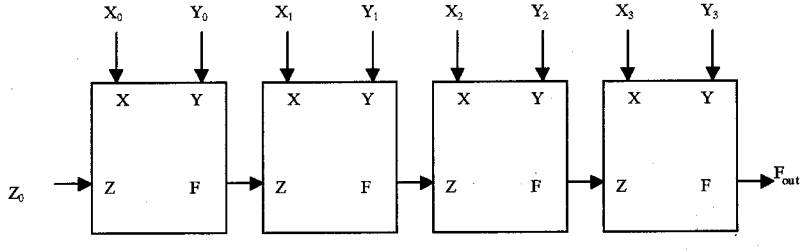
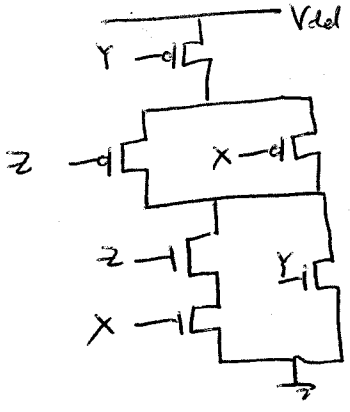


FIG. 2 CMOS circuit



1 ① Since Z is always the last input, move Z closer to outputs:—



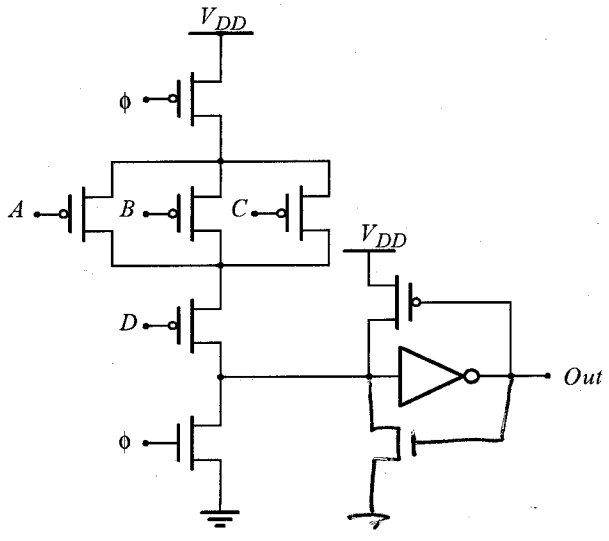
1 ② Increase paths of transistors in the paths containing Z.

½ ③ Progressively sizing X input in PDN; Y input in PUN.

½ ④ PUN sizing

b. What is the potential problem with the circuit shown below? Add or change ONE transistor to remedy the problem.

2



Problem:

Level restoring PMOS does not help charge sharing for the PUN. We need to add an NMOS to drain the potential charge.

Other Partial Credits Problems

$\frac{1}{2}$: Increased delay due to fighting NMOS/PMOS

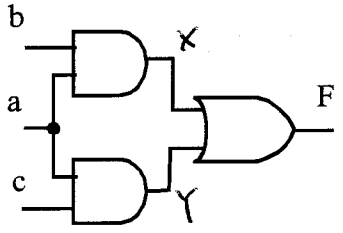
1 : Charge Sharing

Other Solutions:

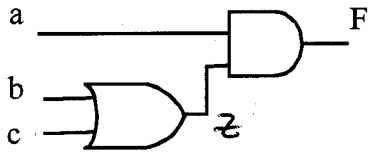
1 : Static NMOS bleeder

3. Power dissipation

The two circuits shown in FIG. 3 (obviously) perform the same logic function. Assume that the gates are implemented (somehow) using complimentary CMOS logic, and that all the nodes in the network have the same capacitance C. The input signals have the following probabilities of being "1": $P_a = 0.1$, $P_b = 0.5$, and $P_c = 0.5$. Determine which implementation consumes the least power and why. Be precise.



Circuit 1



Circuit 2

FIG. 3 Logic Circuits

Both circuits have equivalent logic

$\Rightarrow$ Switching probabilities @ F are the same

$\therefore$ Consider only input nodes.

$P(X=1) = P_a P_b = 0.05$

1.5

$P(Y=1) = P_a P_c = 0.05$

$P_{0\to1}(X) = P_{0\to1}(Y)$

$= 0.05(1-0.05)$

$= 0.0475$

1.5

$P(Z=0) = (1-P_b)(1-P_c) = \frac{1}{4}$

$P_{0\to1}(Z) = \frac{3}{4}\cdot\frac{1}{4} = 3/16$

Circuit with lowest power dissipation:	1

1

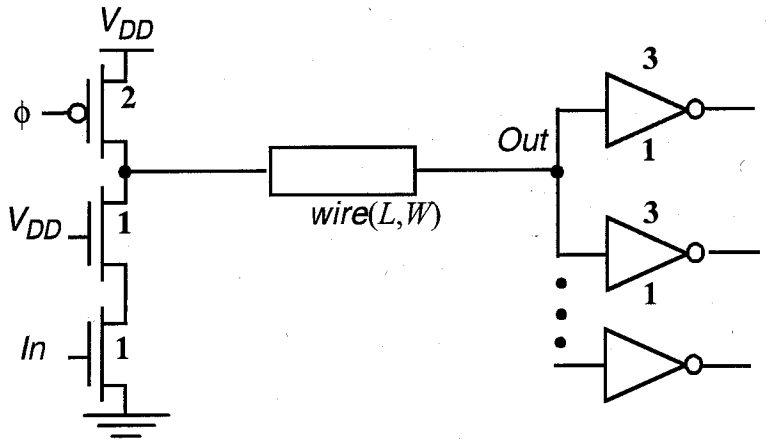
Why: Combined power of internal nodes :-

Ckt 1: $CV_{dd}^2 f (2 \times 0.0475)$

Ckt 2: $CV_{dd}^2 f (3/16)$

Ckt 1 has less power consumption

4. Wiring



A dynamic 2-input NAND gate drives a wire of length L and width W, connecting to a fanout of F identical static CMOS inverters (Figure 1). Assume the following parameters:

FIG. 4 Digital circuit. The numbers annotated indicate the W/L ratios of the transistors

NMOS transistor (per unit width): R_n; $C_{gn} = 2C_t$; $C_{dn} = C_{sn} = C_t$

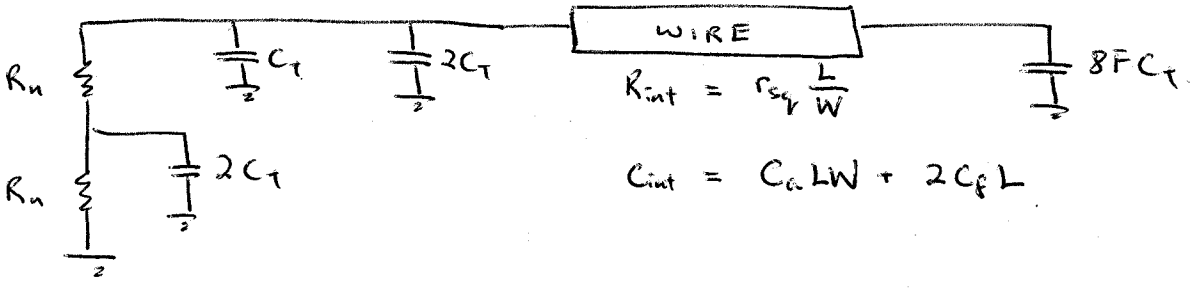
PMOS transistor (per unit width): $R_p = 3R_n$; $C_{gp} = 2C_t$; $C_{dp} = C_{sp} = C_t$;

(these are the only transistor capacitors you should consider, and all of them are from terminal to ground)

Wire parameters: r_{sq} (sheet resistance); c_a (area capacitance per unit area); c_f (fringe capacitance per unit length)

a. Draw the equivalent circuit diagram that you plan to use to determine the propagation delay of the circuit for a 0 -> 1 transition on *In* (assuming ϕ is high). Indicate all important elements (capacitances and resistances) and provide expressions for their values.

2



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b. Derive a symbolic expression for the propagation delay of the network between *In* and *Out* for a 0-to-1 transition at *In*.

t_p Wire Delay $= 0.38\, R_{int} C_{int}$

Using Elmore's Delay model.

$$t_p = 0.69 \{ R_n(2C_T) + 2R_n(C_T + 2C_T) + 2R_n(C_{int}) + (2R_n + R_{int})(8FC_T) \} + \text{Wire Delay}$$

$$= 0.69 (4R_nC_T + 2R_nC_T + 2R_nC_{int} + 16R_nFC_T + 8R_{int}FC_T) + 0.38 R_{int}C_{int}$$

2

c. Assume that all transistors in the NMOS pull-down network have the same width. Determine the absolute minimum value of the propagation delay that can be obtained by the sizing of the transistors in the pull-down network of the NAND gate.

Can size width of NMOS infinitely large

$R_n \rightarrow 0$

but R_nC_T remains constant for NMOS.

Note that one of the $2R_nC_T$ terms above is contributed by PMOS transistor, which does not scale $\Rightarrow$ $2R_nC_T \rightarrow 0$

$$\text{Min. } t_p = 0.69 (4R_nC_T + 8FC_{int}C_T) + 0.38 R_{int}C_{int}$$

d. Alternatively, assume that we would try to reduce the propagation delay by increasing the wire width. Determine the absolute minimum propagation delay that can be obtained that way.

All the terms in answer to part (b) remain constant except

$$0.69\left(2R_nC_{int} + 8FR_{int}C_f\right) + 0.38R_{int}C_{int}$$

As we increase width of wire, area capacitance will dominate over fringe cap.

$$C_{int} = C_aWL + 2C_fL \longrightarrow C_aWL$$

Therefore $R_{int}C_{int} = \left(r_{sq}\frac{L}{W}\right)(C_aWL) \longrightarrow$ Constant.

What remains is the term

$$0.69\left(2R_nC_aWL + 8Fr_{sq}\frac{L}{W}C_f\right)$$

Min. when the 2 terms are equal:-

$$2R_nC_aWL = 8Fr_{sq}\frac{L}{W}C_f$$

$$W = \sqrt{\frac{8Fr_{sq}LC_f}{2R_nC_aL}}$$

Min. delay occurs when W set as above.