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EECS 141: FALL 98 —FINAL

For all problems, you can assume the following transistor parameters:

NMOS:

$V_{Tn} = 0.75V$, $k'_n = 20\ \mu A/V^2$, $\lambda = 0$, $\gamma = 0.5\ V^{1/2}$, $2\Phi_F = -0.6V$

PMOS:

$V_{Tp} = -0.75V$, $k'_p = 7\ \mu A/V^2$, $\lambda = 0$, $\gamma = 0.5\ V^{1/2}$, $2\Phi_F = -0.6V$

NAME	Last First

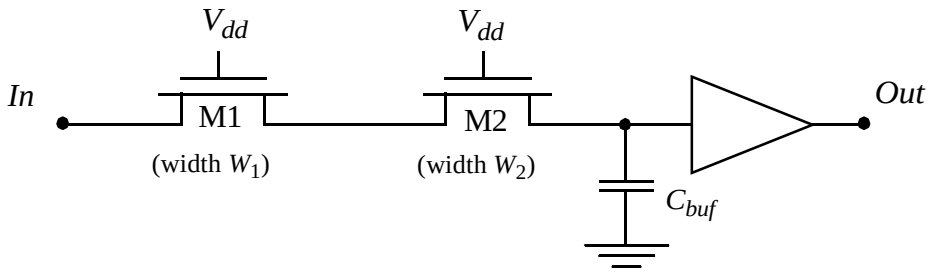
GRAD/UNDERGRAD	

Problem 1:
Problem 2:
Problem 3:
Problem 4:
Problem 5:
Problem 6:

Total	

Problem 1: Logic

Assume that the following network is part of a pass-transistor network. You may assume that the switches can be modeled by the following parameters: $R_{on} = R_{eq}/W$, R_{off} = infinity, and $C_{db} = C_{sb} = C_{eq} * W$ (with W the width of the transistor). All other device capacitances can be ignored. The buffer has a delay equal to t_{buf} and an input capacitance equal to C_{buf}.

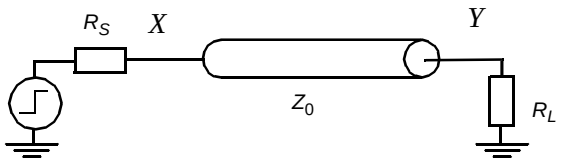


a. Determine the **absolute minimum delay** that can be obtained between input and output through **sizing of the pass-transistors**. Determine under what conditions that minimum is obtained.

b. Assume that $C_{buf} = 2\ C_{eq}$. Propose sizes for the two switches such that the delay of the pass-transistor network (not including the delay of the buffer) is reduced with a factor of **two** compared to the case where both switches are minimum size (W=1). You get extra credit if you can do this with the minimum overall area (= width) for the switches.

PROBLEM 2: Interconnect

Consider the interconnect network shown in the figure below. Assume that a step input of V_{in} ($V(t<0) = 0$ and $V(t>0) = V_{in}$) is applied to the network by a driver with a source resistance equal to R_S. The transmission line is lossless and has a characteristic impedance of Z_0. The line is terminated by with a resistive load with value R_L.



a. Determine the initial voltage at the source (node *X* at t=0) after the step has been applied.

$V_X(t=0)$ =

b. Determine the final voltage at the source (node *X*).

$V_X(t=infinity)$ =

c. Determine the final value at the destination (node *Y*).

$V_Y(t=infinity)$ =

d. Assuming that the following values hold: $R_L = R_S = Z_0/2$, draw the voltage waveforms at nodes X and Y for the first three times-of-flight. Indicate the signal values on the chart.

e. Answer the following questions:

- Will etching the dielectric material away and replacing it with air help to improve the performance of the interconnect network, and why? (assume that the circuit parameters are appropriately adjusted to the changing conditions)

Yes / No

- Assume that the original wire is implemented in Copper. Determine qualitatively if replacing the wiring material with Aluminum would hurt the performance and when this would happen?

- Assume that the driver at the source of the interconnect line is a CMOS inverter. Similarly, the receiver at the end of the line is a CMOS inverter as well. Determine the preferred solution to minimize the propagation delay and power dissipation (**pick one**):

- ☐ Series termination at the source
- ☐ Series termination at the destination
- ☐ Parallel termination at the source
- ☐ Parallel termination at the destination

PROBLEM 3: Interconnect

Suppose you want to design a 3-stage buffer to drive a 75 pF capacitance. V_{dd}=3V. The first buffer gate is minimum size (in the 1.2 micron technology) and has an input gate capacitance of 20 fF.

a. Determine the sizing of the buffers (6 transistors) to optimize delay.

b. Determine that optimimum propagation delay. You may assume that the propagation delay of the minimum size gate delay loaded by an identical gate equals 175 psec.

t_p=

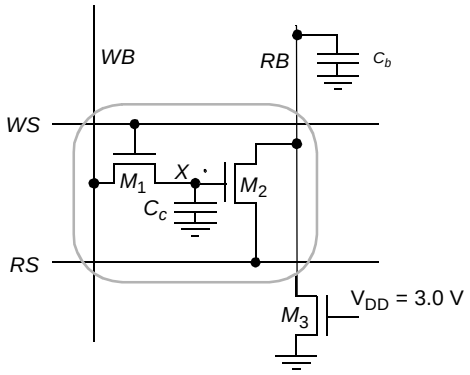
c. Assuming that during the switching the current of an inverter rises linearly to a maximum and then drops back linearly to zero (in a time interval approximately equal to 3.2 times t_p), determine the maximum value of the voltage bounce on the supply rail, assuming that supply rails are connected to the supply with an inductance of 7.5 nH. .

$\Delta V=$

d. One way to reduce the voltage bounce is resizing the buffer. You are allowed to double the propagation delay of the driver to **minimize the bounce**. Describe your strategy, estimate the new sizes of the buffers, and determine the size of the bounce.

PROBLEM 4: Memory

A two-transistor memory cell is shown below. It uses two transistors of identical sizes (M_1 and M_2) with W/L = 2.4/1.2. Separate lines are provided for the read select (*RS*) and write select (*WS*). WS and RS switch between 0 and 3.0 V. You may ignore body effect ($\gamma = 0$) and channel-length modulation ($\lambda = 0$) throughout this problem.



2-T memory cell.

a. Explain the operation of the memory. Draw waveforms for *WB*, *RB*, *WS*, and *RS* for the cases of 1) writing and reading a "1"; 2) writing and reading a "0".

b. Determine the maximum possible current flowing through the cell during a read operation. State clearly your assumptions and simplifications.

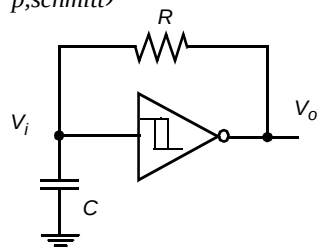
I_{MAX} =

c. Determine the size (W/L) of transistor M_3 so that the voltage swing on the read bit line *RB* never exceeds 1V during a read operation.

W/L =

Problem 5: Sequential Circuits

An astable multivibrator circuit is shown below. The Schmitt trigger is inverting and has a rail-to-rail swing. You may ignore the propagation delay of the Schmitt trigger (or assume that $RC >> t_{p,schmitt}$).



Multivibrator circuit.

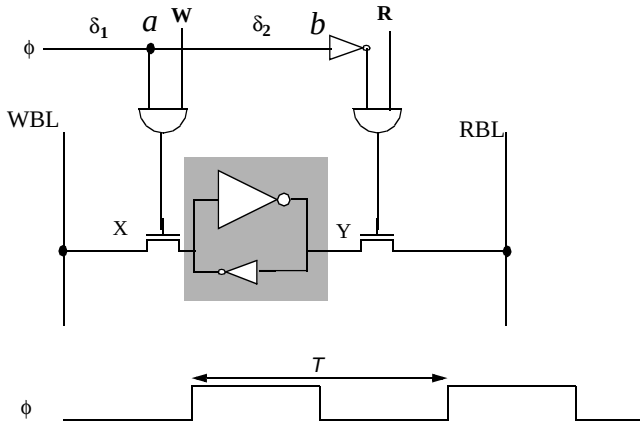
a. Draw the waveforms at the nodes V_i and V_o.

b. Derive an expression for oscillation period as a function of the supply voltage, the Schmitt-trigger thresholds V_{M-} and V_{M+}, and the circuit parameters R and C.

c. Describe what would happen if the Schmitt trigger would be replaced by a simple inverter.

Problem 6. Timing

Consider the two-ported register file cell shown below.



a. The flip-flop highlighted in the Figure consists of a "strong" inverter (large symbol") and a "weak" one. Explain what this means and why this design decision was made.

b. Determine qualitatively the **setup time** of the flip-flop highlighted in the Figure as a function of the important design parameters (i.e. gate delays, rc-delays, etc).

c. Determine qualitatively the **propagation delay** of the flip-flop as a function of the dominant design parameters.

d. The clock experiences a nominal skew δ_1 from the clock generator to point *a* (at the input of the flip-flop), and a nominal skew of δ_2 from the clock generator to node *b* (see Figure).

- Describe qualitatively under what circumstances the clock skew will cause a problem.

- Determine the maximum values of δ_1 and δ_2 so that the circuit will still be operational. You may assume the following design parameters: t_{and} and t_{inv} are respectively the nominal propagation delays of the AND and inverter gates on the clock lines, while t_{pFF} and t_{sFF} are the nominal propagation delay and the set-up time of the flip-flop. It is also known that the clock skew can vary over 15% with respect to its nominal value (due to process variations), while the delays of the gates and the flip-flops can vary with 10%.

δ_{1max}=
δ_{2max}=

e. Ascertain the minimum clock period, T_{min}, as a function of the skew and the gate parameters.

T_{min}=