EECS 141: FALL 2009—MIDTERM 2

For all problems, you can assume that all transistors have a channel length of 100nm and the following parameters (unless otherwise mentioned):

**NMOS:**
$V_{Tn} = 0.2V, \mu_n = 400 \text{ cm}^2/(\text{V} \cdot \text{s}), C_{ox} = 1.125 \text{ } \mu\text{F/cm}^2, v_{sat} = 1e7 \text{ cm/s}, \lambda = 0$

**PMOS:**
$|V_{Tp}| = 0.2V, \mu_p = 200 \text{ cm}^2/(\text{V} \cdot \text{s}), C_{ox} = 1.125 \text{ } \mu\text{F/cm}^2, v_{sat} = 1e7 \text{ cm/s}, \lambda = 0$

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Problem 1: _____ / 14
Problem 2: _____ / 30
Problem 3: _____ / 14
Total: _____ / 58
PROBLEM 1. (14 pts) Wires and Delay

For this problem, you should assume that all of the transistors are minimum channel length (L=0.1µm) and have the following characteristics: $C_G = 2\, \text{fF/µm}$, $C_D = 1\, \text{fF/µm}$, and $R_{sqp} = R_{sqp}/2 = 15\, \text{kΩ/□}$. For the wires, you should assume that $C_{wpp} = 0.1\, \text{fF/µm}^2$, $C_{wfringe} = 0.05\, \text{fF/µm/edge}$, and $R_{sqw} = 0.1\, \text{Ω/□}$

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{circuit_diagram.png}
\end{figure}

a) **(8 pts)** What is the ramp delay of the circuit shown above from In to Out$_1$?
b) (6 pts) Now let’s assume that this circuit is actually a part of the chip’s clock distribution network, and hence we want to make sure that for any value of \( V_{DD} \), the delay from In to Out\(_1\) is always exactly the same as the delay from In to Out\(_2\). Draw a new circuit that achieves this goal; you can modify anything in the original circuit except for the values of \( C_{L1} \) and \( C_{L2} \) and the total length of the wires (i.e., \( L_1 + L_2 = 3\text{mm} \)).
PROBLEM 2. (30 pts) Decoder Energy-Delay Tradeoffs.

This problem will deal with the final decoder circuit shown below. This final decoder is used inside of a 32x32 SRAM, where A and B are outputs from the predecoders. Throughout this problem you can assume that $C_G = 2fF/\mu m$, $C_D = 0$, $R_{sqn} = R_{sqp}/2 = 10k\Omega$, and that the transistors are long-channel from the standpoint of calculating logical effort, and that subthreshold leakage current is negligible.

![Decoder Circuit Diagram]

a) (6 pts) In units of $t_{inv}$ and as a function of $W_1$, $W_2$, and $C_{wl}/C_G$, what is the delay of the final decoder from A or B rising to WL rising?
b) (11 pts) Assuming that the SRAM operates at a clock frequency of $f$, what is the average power consumed by this final decoder? You do not need to include the power consumed by driving the A, B, and En inputs, and you can assume that the En signal is a clock, but that it is only high 20% of the clock cycle. For simplicity you can also assume that the $V_{OL}$ of the ratioed gate is ~0V, and that the $I_{DSAT}$ of a PMOS transistor is equal to $V_{DD}/(R_{eq}*L/W)$. 
c) (6 pts) With \( f = 1 \text{GHz} \), \( W_1 = 2 \mu \text{m} \), \( W_2 = 2 \mu \text{m} \), and \( C_{WL} = 50 \text{fF} \) and as a function of \( V_{DD} \) and \( t_{inv} \), what are the sensitivities \( S_{W1} \) and \( S_{W2} \), where \( S_x = (\partial \text{Power}/\partial x)/(\partial \text{Delay}/\partial x) \)?
d) (7 pts) If you wanted to decrease the power consumption of the final decoder while maintaining the same delay, how would you modify the sizing of the gates? Please be as specific as possible and be sure to explain your answer.
PROBLEM 3. Scaling (14 points)

You recently designed a microprocessor in a 65nm technology with $V_{DD} = 1.2\, \text{V}$ and $V_T = 0.35\, \text{V}$ that runs at 2GHz and consumes a total power of 1W, where 750mW is dynamic power and 250mW is due to subthreshold leakage. In this problem we will look at some of the choices available to us if we were to scale the design to a 45nm technology. Throughout the problem, you should assume that leakage current is modeled by $WI_0e^{(-Vc/38\, \text{mV})}$, where $I_0$ is the same in both the 65nm and 45nm technologies.

a) (7 pts) Using the full scaling model and assuming velocity saturated devices, what would be the new operating frequency, supply voltage, and power consumption of the chip in the 45nm technology?
b) **(7 pts)** Now let’s assume that in moving to the 45nm technology we leave $V_{DD} = 1.2V$ and $V_T = 0.35V$. Still with velocity saturated devices and assuming that $\xi_{crit} = 5V/\mu m$, now what is the new operating frequency and power consumption of the chip?