For all problems, you can assume that all transistors have a channel length of 100nm and the following parameters (unless otherwise mentioned):

**NMOS:**
\[ V_{Tn} = 0.2\, \text{V}, \, \mu_n = 400\, \text{cm}^2/(\text{V} \cdot \text{s}), \, C_{ox} = 1.125\, \mu\text{F/cm}^2, \, v_{sat} = 1\times10^7\, \text{cm/s}, \, \lambda = 0 \]

**PMOS:**
\[ |V_{Tp}| = 0.2\, \text{V}, \, \mu_p = 200\, \text{cm}^2/(\text{V} \cdot \text{s}), \, C_{ox} = 1.125\, \mu\text{F/cm}^2, \, v_{sat} = 1\times10^7\, \text{cm/s}, \, \lambda = 0 \]

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Problem 1: _____ / 18

Problem 2: _____ / 20

Problem 3: _____ / 26

Total: _____ / 64
PROBLEM 1. (18 pts) Complex Gates and Elmore Delay.

a) **(6 pts)** Implement the function $F = (A \cdot B + C) \cdot (D+E)$ with a complex static CMOS gate. Assuming $R_{sgp} = 3R_{sqn}$, you should size your gate so that the worst-case pull up resistance is equal to the worst-case pull-down resistance.
b) **(6 pts)** Using the switch model for the transistors, draw the RC network you would use to calculate the delay of the gate shown below when \( B = V_{DD}, \ C = 0V, \) and \( A \) transitions from \( 0V \) to \( V_{DD} \). You can assume that \( C_G = C_D = 2fF/\mu m, \ R_{sxn} = 10k\Omega/\square, \) and \( R_{sqp} = 30k\Omega/\square. \)
c) (6 pts) Using the same model and component values you drew in part b), what is the delay of the gate under the same situation (i.e., when \(B = V_{DD}, C = 0V\), and \(A\) transitions from 0V to \(V_{DD}\))? You should provide your answer for the delay in both absolute ps and in units of \(t_{inv}\). For your convenience the gate has been repeated below.

![Diagram of the gate with component values](image-url)
PROBLEM 2. (20 pts) IV Characteristics, VTCs, and Energy

a) **(2 pts)** For a long-channel (quadratic) NMOS transistor with $V_{GS} = V_{DS} = 1.2V$, how does the drain current change if the mobility of the device $\mu_n$ is doubled? How about if $C_{ox}$ is doubled?

b) **(6 pts)** Now let’s look at a short-channel (velocity-saturated) NMOS transistor with $V_{GS} = V_{DS} = 1.2V$. Using the velocity saturated model for this transistor, how much drain current would you get from a 1µm wide transistor if you doubled $\mu_n$ to 800 cm²/(V·s)? How about if you doubled $C_{ox}$ to 2.25 µF/cm²?
c) *(6 pts)* For parts c) and d), you should use the simple switch model of the transistors with $R_{sqn} = 10\, \Omega$, $R_{sqp} = 20\, \Omega$, $V_{DD} = 1.2\, \text{V}$, and $V_{TN} = |V_{TP}| = 0.2\, \text{V}$. Draw the VTC of the circuit shown below and provide the values of $V_{OH}$, $V_{OL}$, $V_{IH}$, and $V_{IL}$. 

![Circuit Diagram]
d) **(6 points)** For this same circuit (repeated below), how much energy is supplied by $V_{DD}$ to charge $C_L$ when In steps from $V_{DD}$ to 0V?
PROBLEM 3. Logical Effort and Gate Sizing (26 points)

a) (6 pts) What is the path effort from In to Out?

b) (2 pts) What EF/stage minimizes the delay of this chain of gates?

c) (8 pts) Size the gates to minimize the delay from In to Out.

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<tr>
<th>Size</th>
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d) (4 pts) By changing only the order (but not the types) of the gates, can you reduce the total capacitance of the gates in this chain? If so, draw the re-ordered chain (you do not need to recalculate the sizes) and explain why the capacitance is reduced; if not, explain why this isn’t possible.
e) **(6 points)** While maintaining the same logical functionality and without changing $C_{in}$, can you improve the delay of this chain of gates (repeated below) by changing the number and/or types of gates? Please draw an improved schematic for the new chain of gates; you don’t need to provide gate sizes.

Original chain:

![Original Chain Diagram]

Improved chain: