For all problems, you can assume that all transistors have a channel length of 100nm and the following parameters (unless otherwise mentioned):

**NMOS:**
- \( V_{Tn} = 0.2 \text{V} \)
- \( \mu_n = 400 \text{ cm}^2/(\text{V} \cdot \text{s}) \)
- \( C_{ox} = 1.125 \mu \text{F/cm}^2 \)
- \( v_{sat} = 1 \times 10^7 \text{ cm/s} \)
- \( L = 100 \text{nm} \)
- \( \gamma = \lambda = 0 \)

**PMOS:**
- \( |V_{Tp}| = 0.2 \text{V} \)
- \( \mu_p = 200 \text{ cm}^2/(\text{V} \cdot \text{s}) \)
- \( C_{ox} = 1.125 \mu \text{F/cm}^2 \)
- \( v_{sat} = 1 \times 10^7 \text{ cm/s} \)
- \( L = 100 \text{nm} \)
- \( \gamma = \lambda = 0 \)

### NAME

Last Solutions First

### GRAD/UNDERGRAD

Problem 1: ____/ 16

Problem 2: ____/ 14

Problem 3: ____/ 24

Problem 4: ____/ 24

Problem 5: ____/ 18

Total: ____/ 96
PROBLEM 1: Logic Styles and LE (16 pts)

For this problem, you can assume that $C_G = C_D = 2fF/\mu m$, $R_{sqn} = 10k\Omega/\Box$, $R_{sqp} = 20k\Omega/\Box$, and that the transistors are quadratic (i.e., long-channel).

a) (3 pts) What logical function does the gate shown below implement?

\[ \text{Out} = (A + \overline{B}) \cdot C \]

b) (7 pts) Given the sizing shown below, what value of W would you use in order to make the worst-case LE of the C input equal to half the LE of the A and B inputs (i.e., $\text{LE}_C = \frac{1}{2}\text{LE}_A$)? What would be the LE of the C input in this case?

\[ \text{LE}_C = \frac{(\frac{1}{2} + \frac{1}{2} + 1) R_{sq} L \cdot 2 C_g}{R_{sq} L \cdot 3 C_g} \]

Note that the worst-case resistance of the stage is the same regardless of whether we are looking at the C, B, or A inputs. So, Cin for C must be 1/2 the Cin for A or B:

\[ W = 1 \]

\[ \text{LE}_C = \frac{4}{3} \]
c) **(6 pts)** During evaluation, what is the logical effort of the dynamic gate shown below from input In?

\[ R_{\text{pullup}} = \frac{R_{\text{pullup}}}{R_{\text{inv}}} \cdot \left( 1 + \frac{1}{4} \right) = 2.5 \]

\[ R_{\text{keeper}} = \frac{1}{0.2} = 5 \]

\[ I_{\text{pullup}} \propto \frac{1}{2.5} - \frac{1}{5} = \frac{1}{5} \rightarrow R_{\text{gate}} = 5 \]

\[ C_{\text{gate}} = 1 \]

\[ LE = \frac{R_{\text{gate}} C_{\text{gate}}}{R_{\text{inv}} C_{\text{inv}}} = \frac{5}{3} \]
PROBLEM 2: SRAM Design (14 points)

For this problem you should use the velocity saturated transistor model.

a) (8 pts) Shown below is an SRAM cell during a read, where the power supply of the SRAM has been reduced to 0.65V while the V_{DD} of the wordline is 1.2V. Note that the bitlines have also been precharged to 0.65V. With the device sizing shown below, what is the read $\Delta V$? (Hint: How much larger is $I_{DSAT}$ for a transistor with $V_{GS} = 1.2V$ than with $V_{GS} = 0.65V$?)

\[ E_cL = \frac{2V_{sat}}{\mu} \quad L = 0.5V \quad V_{TN} = 0.2V \]

\[ \frac{I_{DSAT} (V_{GS} = 1.2V)}{I_{DSAT} (V_{GS} = 0.65V)} = \frac{(1.2V - 0.2V)^2}{(1.2V - 0.2V + 0.5V)} \approx 3.13 \]

So, even though access device is hault as wider, its current would be higher than the pull-down device if $\Delta V \approx 0$. So, lets guess that both are in sat:

\[ \frac{1}{2} \left( \frac{1.2V - \Delta V - 0.2V}{1.2V - \Delta V - 0.2V + 0.5V} \right)^2 = \frac{(0.65 - 0.2V)^2}{(0.65 - 0.2V) + 0.5V} \rightarrow [\Delta V \approx 278mV] \]

Check our guess:

\[ V_{0\text{access}} = 1.2V - 278mV - 200mV = 722mV \]
\[ V_{0\text{access}} = 0.65V - 278mV = 372mV \]
\[ V_{CT\text{pd}} = 0.65V - 0.2V = 450mV \]
\[ V_{0\text{pd}} = 278mV \]

\[ V_{0\text{access}} = \frac{722mV - 500mV}{722mV - 500mV} \approx 295mV \]
\[ V_{0\text{pd}} = \frac{0.45V - 0.5V}{0.45V - 0.5V} \approx 237mV \]
b) *(6 pts)* Assuming that in your answer to part a) you calculated that the pull-down device is saturated, how much faster does the SRAM cell pull down the bitline when the wordline is driven to 1.2V compared to if the wordline was driven to only 0.65V? (Note that most of the credit on this problem will be given for finding the right regions of operation and setting up the equations.)

\[
\text{When } WL = 1.2V: \\
I_{\text{pull-down}} = I_{\text{DSAT}} \quad \text{of the pull-down device} \\
I_{\text{pull-down}} \propto 0.24 \cdot \frac{(0.65V - 0.2V)^2}{(0.65V - 0.2V) + 0.5V}
\]

\[
\text{When } WL = 0.65V: \\
\begin{align*}
0.65V & \quad \text{pull-down much bigger, so it should} \\
0.12 & \quad \text{be in linear region.} \\
0.24 & \quad \text{=} \quad 0.65V \\
\end{align*}
\]

**Solve for \( \Delta V \):**

\[
\frac{0.12 \text{mm} \cdot 1 \text{cm/s}}{0.65V - 0.2V - \Delta V + 0.5V} = 0.24 \text{mm} \cdot 100 \text{cm}^2/\text{Vsec} \frac{0.65V - 0.2V - \Delta V/2}{\Delta V}
\]

\[
\Rightarrow \quad \Delta V \approx 52 \text{ mV}
\]

\[
\frac{I_{\text{pd}}(WL=1.2V)}{I_{\text{pd}}(WL=0.65V)} = \frac{0.24 \cdot (0.65V - 0.2V)^2}{0.12 \cdot (0.65V - 0.2V - 0.052V)^2} \\
= \frac{(0.65V - 0.2V)^2}{(0.65V - 0.2V + 0.5V)} \\
\frac{I_{\text{pd}}(WL=1.2V)}{I_{\text{pd}}(WL=0.65V)} \approx 2.417
\]
**PROBLEM 3: Dynamic Logic Design (24 pts)**

For this problem, you can assume that $V_{DD} = 1.2V$, $C_G = 2fF/\mu m$, and $C_D = 1fF/\mu m$.

a) **(6 pts)** In the domino gate shown below, what is the minimum $W_n$ necessary to ensure that the gate does not fail due to charge sharing? You can assume that with the sizing shown, the $V_{IH}$ of the inverter is $\frac{3}{4}V_{DD}$, and that none of the source/drain regions have been shared.

```
CLK --- 1um --- Out
A 1um
B 1um
CLK 1um
```

**Cap on node X:**

$$C_X = C_{DG} + C_{DA} + C_{GA}$$

$$= 3\mu m \cdot 1fF/\mu m + 1\mu m \cdot 2fF/\mu m$$

$$= 5fF$$

**Cap on node Out:**

$$C_{Out} = C_{DA} + C_{DPre} + 5W_n C_G$$

$$= 2fF + 10fF/\mu m \cdot W_n$$

**Charge sharing:**

$$V_{DD} \cdot C_{Out} = V_{new} (C_{Out} + C_X)$$

$$V_{new} = \frac{C_{Out}}{C_{Out} + C_X} \cdot V_{DD}$$

To meet $V_{IH}$ of inverter:

$$V_{new} > \frac{3}{4} V_{DD}$$

$$\frac{2fF + 10fF/\mu m \cdot W_n}{2fF + 10fF/\mu m \cdot W_n + 5fF} > \frac{3}{4}$$

$$2fF + 10fF/\mu m \cdot W_n \geq \frac{5.25 \cdot ff + 7.5 \cdot ff/\mu m \cdot W_n}{W_n \geq 1.3 \mu m}$$
b) \((6 \text{ pts})\) Other than changing \(W_n\), the sizes of the transistors in the dynamic gate, or adding a keeper, what else can change in the gate from part a) in order to mitigate the charge sharing issue? You should explain your changes and draw a new transistor-level schematic of the gate (no sizing necessary). To receive full credit on this problem, you should identify two independent changes; if you identify three changes you will receive bonus credit.

1. **Pre-charge the internal node:**

   \[
   \text{clk-}d \quad \text{clk-}b \quad \text{clk-}c \quad \text{clk-}a
   \]

2. **Re-order the gate to increase \( \overline{C_{out}} \):**

   \[
   \text{clk-}d \quad \text{clk-}b \quad \text{clk-}c \quad \text{clk-}a
   \]

3. **Reduce the skew of the inverter to decrease \( V_{IH} \) (doesn’t reduce charge sharing, but reduces its impact on the output):**

   \[
   \text{clk-}d \quad \text{clk-}b \quad \text{clk-}c \quad \text{clk-}a
   \]
c) **(2 pts)** On the evaluation edge, what is the delay of the dynamic gate shown below as a function of $R_{sq,n}$, $C_L$, $W$, and $W_{clk}$? You can assume that $C_D = 0$ and ignore slope effect.

![Diagram of dynamic gate](attachment:dynamic_gate_diagram.png)

$$t_p = \ln(2) R_{sq,n} \cdot L \cdot \left( \frac{1}{W} + \frac{1}{W_{clk}} \right) \cdot C_L$$

**d) ****(2 pts)** Assuming that $I_n$ has an activity factor of $\alpha_{0\rightarrow 1}$, how much power is consumed due to driving $I_n$? How about due to driving $clk$? You should provide your answers in terms of $W$, $W_{clk}$, $\alpha_{0\rightarrow 1}$, $C_G$, $V_{DD}$, and $f$.

$$P_{I_n} = \alpha_{0\rightarrow 1} C_G \cdot W \cdot V_{DD}^2 / f$$

$$P_{clk} = C_G (W_{clk} + 1) \cdot V_{DD}^2 / f$$
e) (8 pts) Increasing the size of the evaluation transistor (i.e., increasing $W_{clk}$) speeds up the dynamic inverter, but costs power. Using the results from parts c) and d), can you find an optimal $W_{clk}/W$?

"Optimal" here can only mean that we are spending just the right amount of power for a given delay (or hitting the best delay for a given power). That means we should be looking at sensitivities of $W$ and $W_{clk}$ and trying to balance them.

\[
\frac{\Delta P}{\Delta W} = \frac{-1}{2} n^2 (R_{s_{nW}}L_{C_L}) \quad \text{or} \quad \frac{\Delta P}{\Delta W_{clk}} = \frac{-1}{2} n^2 (R_{s_{nW}}L_{C_L})
\]

\[
\frac{\Delta P}{\Delta W} = \alpha_{0-1} C_g V_{eo}^2 \quad \text{or} \quad \frac{\Delta P}{\Delta W_{clk}} = C_g V_{eo}^2
\]

\[
\Delta W = \frac{-\alpha_{0-1} C_g V_{eo}^2}{n^2 (R_{s_{nW}}L_{C_L})} \quad \text{or} \quad \Delta W_{clk} = \frac{-C_g V_{eo}^2}{n^2 (R_{s_{nW}}L_{C_L})}
\]

\[
\Delta W = \Delta W_{clk}
\]

\[
\left(\frac{C_g V_{eo}^2}{n^2 (R_{s_{nW}}L_{C_L})}\right) \alpha_{0-1} W^2 = \left(\frac{C_g V_{eo}^2}{n^2 (R_{s_{nW}}L_{C_L})}\right) W_{clk}^2
\]

\[
\frac{W_{clk}}{W} = \sqrt[2]{\alpha_{0-1}}
\]
PROBLEM 4: Timing and Clock Distribution (24 points)

In this problem we will be examining the pipeline shown below. The minimum and maximum delays through the logic are annotated on the figure, and the flip-flops have the following properties: $t_{clk-q} = 50\text{ps}$, $t_{setup} = 25\text{ps}$, and $t_{hold} = 25\text{ps}$. You can assume that the clock has no jitter.

![Diagram of pipeline with flip-flops and delays](image)

a) (6 pts) What is the minimum clock cycle time for this pipeline? Are there any minimum delay violations?

**Min. cycle:** $CL_1$ has largest $tp_{max}$, so:

\[
t_{clk-q} + tp_{max1} + t_{setup} < T_{cycle}
\]

\[
50\text{ps} + 300\text{ps} + 25\text{ps} < T_{cycle}
\]

\[
T_{cycle} > 375\text{ps}
\]

**Min. delay:** $CL_2$ has smallest $tp_{min}$, so:

\[
t_{clk-q} + tp_{min2} > t_{hold}
\]

\[
50\text{ps} + 25\text{ps} > 25\text{ps}
\]

\[
50\text{ps} > 0\text{ps} \checkmark
\]

\[\Rightarrow\text{No hold time problem.}\]
b) (4 pts) Now we’ll include the clock distribution network for this pipeline. Assuming that the delay of each inverter is nominally 50ps, but that each inverter’s delay varies randomly by +/-20%, now what is the minimum clock cycle time?

Each inverter delay varies by ±10ps. CL1 has largest max delay, but since only picks up skew from inverters D and E (whereas path through CL2 has skew from B, E, C, and F), need to check which one is the most critical.

\[ t_{p, max_1} + 2\Delta_{inv} = 300\text{ps} + 20\text{ps} = 320\text{ps} \]
\[ t_{p, max_2} + 4\Delta_{inv} = 275\text{ps} + 40\text{ps} = 315\text{ps} \]

So, CL1 is still critical:

\[ t_{clk} + t_{p, max_1} + t_{setup} + 2\Delta_{inv} < T_{cycle} \]

\[ T_{cycle} < 3.95\text{ps} \]
c) (4 pts) Under these same conditions (i.e., 50ps nominal inverter delay, +/-20% delay variation), can this pipeline fail any minimum delay constraints?

Path through CL2 has smallest \( t_{p,\text{min}} \) and most skew, so that's clearly where we need to worry about failure.

\[ \text{clk-\( \downarrow \)} + t_{p,\text{min}2} > \text{thold} + 4 \Delta \text{tmin} \]

50ps + 25ps > 25ps + 40ps

10ps > 0 ps \( \checkmark \)

\( \rightarrow \) No hold time violation.
d) **(10 pts)** If we replace the flip flops by pulsed latches with the same $t_{\text{clk-q}}$, $t_{\text{setup}}$, and $t_{\text{hold}}$ as the flip-flops, and with $t_{d-q} = t_{\text{clk-q}} + t_{\text{setup}}$, can the minimum cycle time of the pipeline be reduced without potentially failing a minimum delay constraint? If so, how wide must the pulses be, and what is the new minimum cycle time? If not, explain which path fails the minimum delay constraint.

Forward max pulse width without hold time:

\[
\begin{align*}
&t_{\text{clk-q}} + t_{p,\text{min2}} \leq 4\Delta t_{\text{inv}} + T_{\text{on}} + t_{\text{hold}} \\
&T_{\text{on}} \leq 50\text{ps} + 25\text{ps} - 40\text{ps} - 25\text{ps} \\
&T_{\text{on}} \leq 10\text{ps}
\end{align*}
\]
For cycle time, look at worst-case clock with $T_{cw} = 10ps$:

\[ T_{cycle} = 2 \Delta t_{1w} \]

- **polk, l1**
- **polk, l2**
- **polk, l3**

For path through CL1: $t_{l1} + t_{polk, l1} + t_{setup} < T_{cycle} - 2 \Delta t_{1w} + T_{ow}$

\[ T_{cycle} > 385ps \]

Check that path through CL2 is still OK:

\[ t_{l1} + t_{polk, l1} + t_{setup} < T_{cycle} - 2 \Delta t_{1w} \]

\[ 350ps < 365ps \] \[ \checkmark \]

$\Rightarrow$ CL2 OK. (Ok even if $T_{ow}$ be before $L3 \uparrow$)

* If you get the right $T_{cycle}$, you will receive full credit.
* If you check that the CL2 path is still OK under these conditions, you will receive bonus points.
PROBLEM 5: Arithmetic (18 pts)

In this problem we will look at designing a comparator whose output $C_{out} = 1$ whenever $A > B$, where $A$ and $B$ are unsigned binary numbers. Throughout this problem you can assume that you have both the true and complement versions of the inputs available to you.

a) (2 pts) If $A$ and $B$ are both only a single bit, draw a gate-level schematic (i.e., no transistors) showing how you would compute $C_{out}$.

If $A=1$ and $B=0$, $A > B$.

```
  A --> D --> C_{out}
  B
```

b) (5 pts) Now assume that $A$ and $B$ are both two bit numbers – i.e., we have inputs $A_{1:0}$ and $B_{1:0}$. To compare between $A_0$ and $B_0$ we can use the “half comparator” circuit you drew in part a). Draw a gate level schematic showing how you would implement a “full comparator” and use it to calculate the final $C_{out}$.

```
  A --> HC --> C_{out} <==>  A --> D --> C_{out}
  B
```

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C_{out}</th>
<th>C_{in}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
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<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Two-bit comparator:

This can also be replaced with

```
  A_1 --> FC --> C_{out}
  B_1

  A_0 --> HC --> C_0
  B_0
```

(see next page)
c) (5 pts) Notice that these comparators have several characteristics that are very similar to adders. As a function of A and B, define new P (propagate) and G (generate) signals that are appropriate for comparators, and then write the logic equation that gives the C_{out} for a particular bit using P, G, and C_{in}.

Look at truth table again:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C_{out}</th>
<th>P</th>
<th>G</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>C_{in}</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>x</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>C_{in}</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

(Never use intermediate Cout, so it doesn’t matter what P is when C=1)

\[ G = A \cdot \overline{B} \quad P = A + \overline{B} \]

or

\[ P = \overline{A} \cdot \overline{B} + A \cdot B = A \oplus B \]

\[ C_{out} = G \cdot P \cdot C_{in} \]
d) (6 pts) Given your definitions from part c), sketch a block diagram showing how you can implement an 8-bit “carry lookahead” comparator using the PG block shown below.