



EECS 141: FALL 2007—FINAL EXAM

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):

NMOS:

$$V_{Tn} = 0.4, k'_n = 115 \mu\text{A}/\text{V}^2, V_{VSAT} = 0.6\text{V}, \lambda = 0, \gamma = 0.4 \text{ V}^{1/2}, 2\Phi_F = -0.6\text{V}$$

PMOS:

$$V_{Tp} = -0.4\text{V}, k'_p = -30 \mu\text{A}/\text{V}^2, V_{VSAT} = -1\text{V}, \lambda = 0, \gamma = -0.4 \text{ V}^{1/2}, 2\Phi_F = 0.6\text{V}$$

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GRAD/UNDERGRAD	
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Problem 1: ____ / 16

Problem 2: ____ / 21

Problem 3: ____ / 22

Problem 4: ____ / 16

Problem 5: ____ / 14

Total: ____ / 89

PROBLEM 1: SRAM Design (16 pts)

In this problem, we will be looking at a 256 x 256 SRAM, where each 6T cell is 4 μm wide and 3 μm tall. All of the devices in the SRAM cell are minimum length ($L = 0.25\mu\text{m}$), and you can assume that both the NMOS access transistors and the NMOS pull-down transistors are 0.5 μm wide. You can also assume that when $V_{DD} = 2.5\text{V}$, the transistors have $C_G = 2\text{fF}/\mu\text{m}$, $C_D = 1\text{fF}/\mu\text{m}$, and $R_{sqn} = R_{sqp}/2 = 15\text{k}\Omega/\square$.

- a) (2 pts) For $V_{DD} = 2.5\text{V}$, what is the total capacitance loading each bitline in this memory? You can assume that the bitline wire has a capacitance/length of 0.15fF/ μm .

- b) (3 pts) If the supply voltage of the SRAM was reduced to 1.5V, would the effective capacitance on the bitlines increase, decrease, or stay the same? Why?

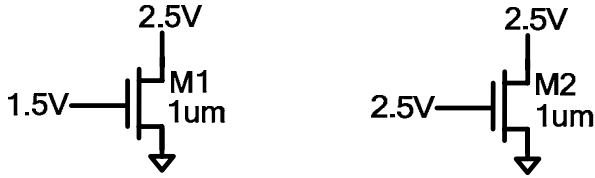
c) (4 pts) Given your answer to part a) (i.e., $V_{DD} = 2.5V$), and assuming that the delay of the final stage in the decoder is 100ps, what is the delay (in ns and including the slope effect) from the wordline rising to the bitline falling?

d) (4 pts) If the memory operates at 100MHz, how much dynamic power is dissipated due to switching the 256 bitlines? You can assume that the bitlines swing all the way from 0V to V_{DD} .

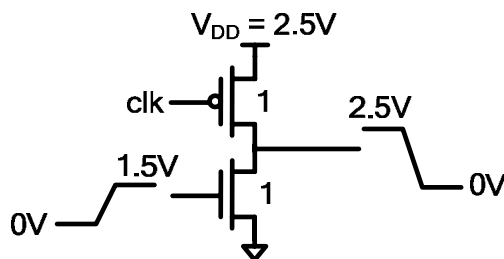
- e) **(3 pts)** Now we'll look at whether we can save some power by adding sense amps to this design. If the sense amps would dissipate 10% of the power you calculated in part d), but the bitlines now swing only between 2V and V_{DD} (=2.5V), will adding sense amps reduce the power of the SRAM? If so, by how much?

PROBLEM 2: Logical Effort and Transistor Models (21 pts)

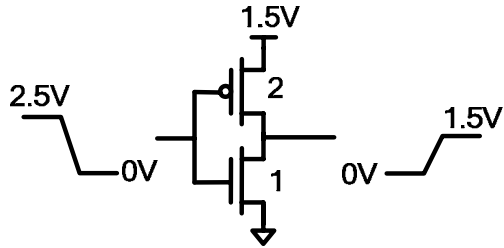
- a) (3 pts) Using the unified transistor model, what is the ratio of drain currents for the two $0.25\mu\text{m}$ long transistors shown below? I.e., what is $I_{DS}(M1)/I_{DS}(M2)$?



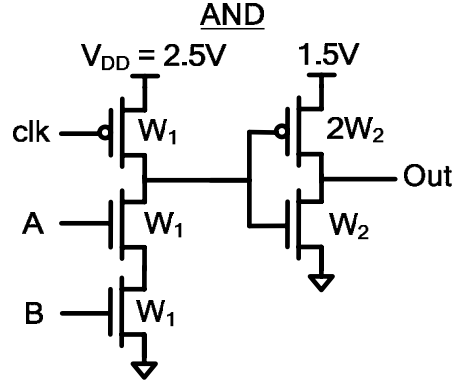
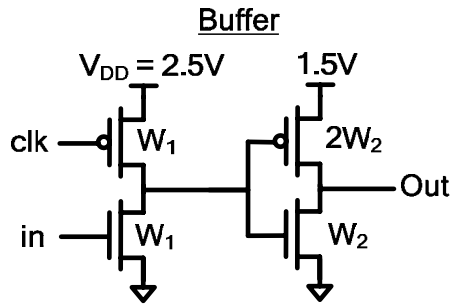
- b) (4 pts) Shown below is a dynamic (unfooted) inverter where the input to the inverter swings only between 0V and 1.5V, while the power supply for the dynamic inverter is 2.5V. During evaluation, what is the logical effort of this dynamic inverter relative to a standard inverter with $W_p = 2W_n$ and $V_{DD} = 2.5\text{V}$? (Hint: your answer to part a) is directly related to this problem.)



- c) (6 pts) Now we'll look at the static inverter (shown below) that would drive the dynamic inverter we just looked at. Once again comparing to a standard inverter with a supply voltage of 2.5V, what is the logical effort of this inverter for the rising transition at the output? (Hint: What is the effective resistance of the PMOS transistor?)

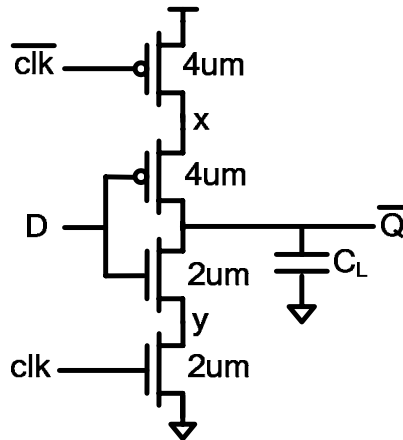


- d) (8 pts) Let's now look at building chains of logic using such "alternating supply" domino gates (as shown below). Assuming your answer to part b) was $LE_{\text{dinv}} = 0.75$ and to part c) was $LE_{\text{inv}} = 1.5$, what is the EF/stage you should target to minimize the delay of a chain of these gates?

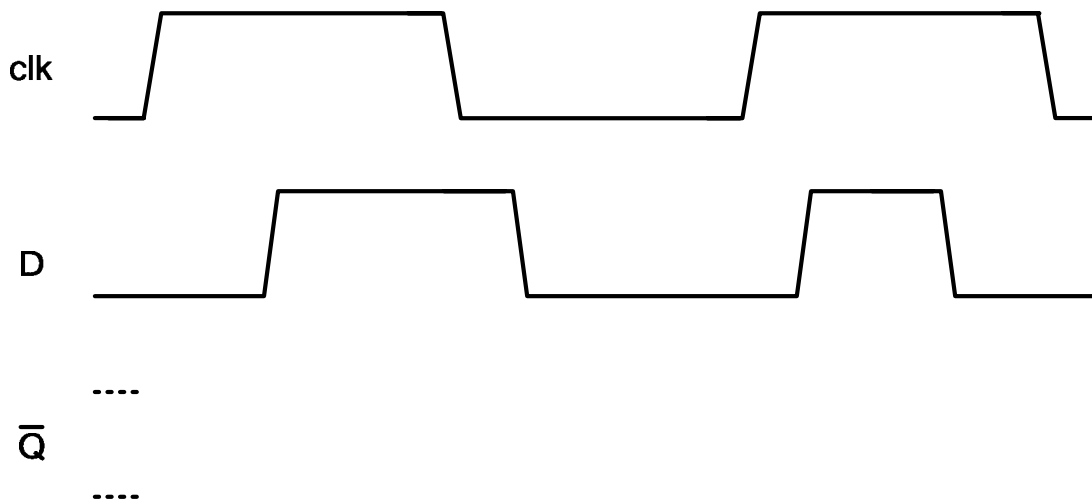


PROBLEM 3: Sequential Elements (22 points)

In this problem we will be examining the latch shown below, which has been implemented out of a tri-state inverter. Throughout this problem, you can assume that $V_{DD} = 2.5V$, $C_G = 2fF/\mu m$, $C_D = 2fF/\mu m$, and $R_{sqn} = R_{sqp}/2 = 15k\Omega/\square$.



- a) (2 pts) Assuming the latch is ideal (i.e., has no delay, zero setup/hold time, etc.), fill in the waveform for \overline{Q} given the clock and data inputs shown below.



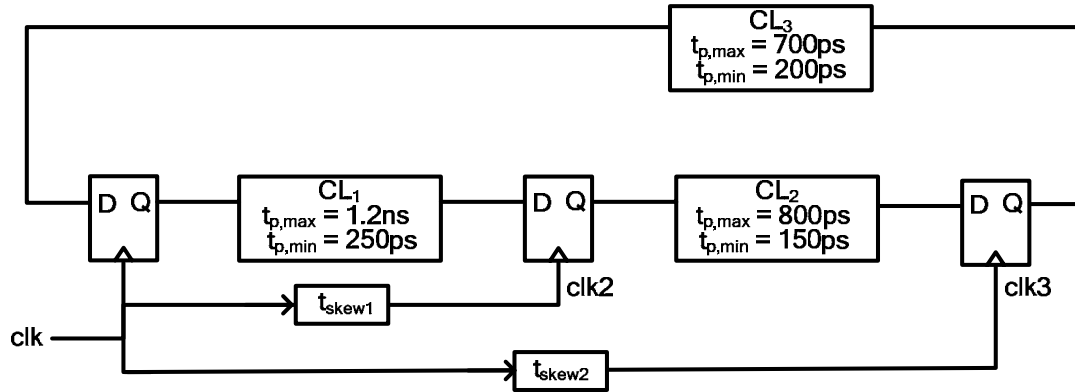
- b) (6 pts)** For $C_L = 50\text{fF}$ and assuming \overline{Q} is initially charged to V_{DD} and y is initially 0V , what is the $t_{\text{clk}\rightarrow\overline{q}}$ of this latch when $D=1$? You should assume that clk is a ramp.

- c) (4 pts) One of your fellow designers comes to you one day and says that when she used this latch in her circuit with $C_L = 5\text{fF}$, the latch failed to function correctly. More specifically, if D transitioned, the inverter receiving the output of the latch would transition even when clk was low. However, you have verified that the latch functions correctly when $C_L = 50\text{fF}$. What is the cause of the error when the latch has a small C_L ? (Hint: Think about the second transition of D.)
- d) (6 pts) What is the minimum load capacitance required for the latch to function correctly? You can assume that the inverter receiving the output of the latch has an ideal VTC with a switch point $V_{sw} = V_{DD}/2$, and that none of the transistors' source/drain regions have been shared.

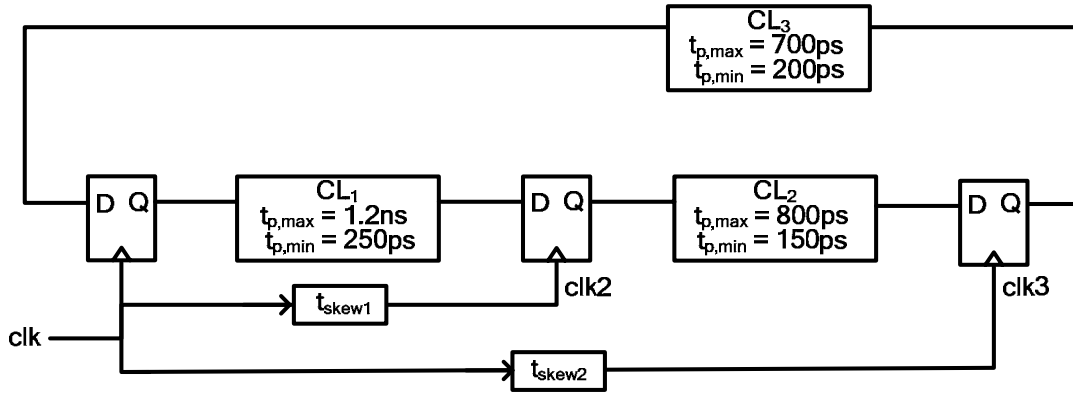
- e) **(4 pts)** Other than artificially increasing C_L , how can you modify the latch to fix the problem you identified in part c)? You should explain your fix and draw a new transistor-level schematic of the latch (no sizing necessary). (Note that there is more than one possible fix – you will receive bonus credit for up to two additional fixes you identify and draw.)

PROBLEM 4: Timing (16 points)

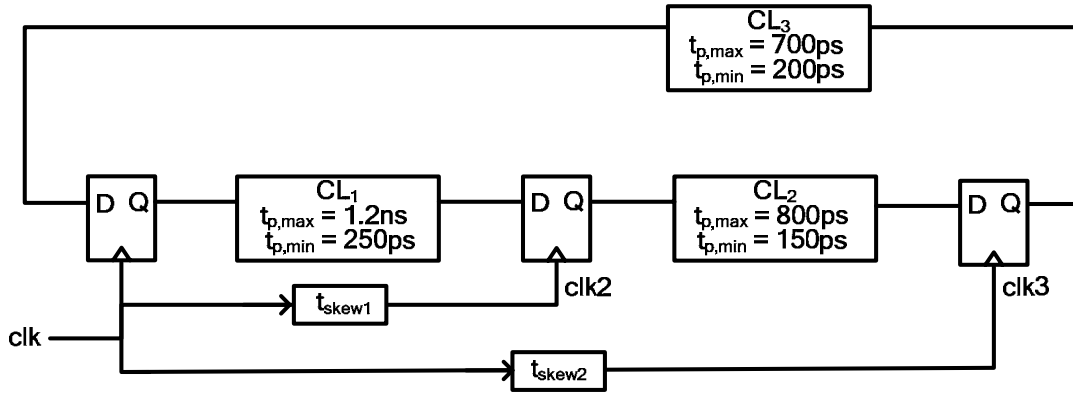
In this problem we will be examining the pipeline shown below. The minimum and maximum delays through the logic are annotated on the figure, and the flip-flops have the following properties: $t_{\text{clk-q}} = 150\text{ps}$, $t_{\text{setup}} = 50\text{ps}$, and $t_{\text{hold}} = 100\text{ps}$. You can assume that the clock has no jitter, but t_{skew1} and t_{skew2} can be either positive or negative.



a) (4 pts) What is the minimum clock cycle time if $t_{\text{skew1}} = -100\text{ps}$ and $t_{\text{skew2}} = 50\text{ps}$?



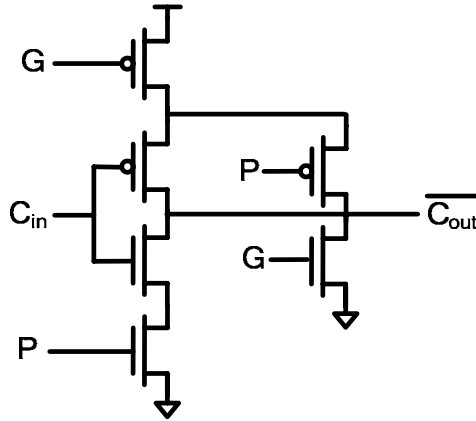
- b) (4 pts) Assuming t_{skew2} is fixed at 50ps, how negative can t_{skew1} be before this pipeline (repeated above for your convenience) fails a hold-time constraint?



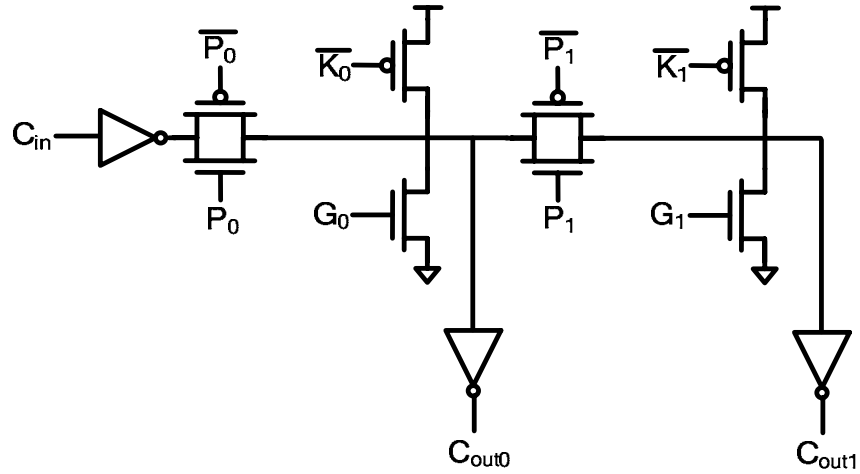
- c) (8 pts) If you could intentionally set the values of t_{skew1} and t_{skew2} , what values would you choose in order to minimize the cycle time of this pipeline (again repeated above)? What would be the cycle time in this case?

PROBLEM 5: Arithmetic Blocks (14 points)

- a) (3 pts) Shown below is a static CMOS implementation of a gate that computes the carry-out at a particular bit position. If the “P” signal that was fed into this gate was calculated using $A + B$ (instead of $A \oplus B$), would the output of this gate still be correct? Why or why not?



- b) (5 pts) Now let's look at a the gate shown below that computes the carry-out for two bit positions, but this time implemented with a Manchester carry chain. Is this gate guaranteed to function correctly if the P signals that are fed to this gate are calculated as $A + B$? Why or why not?



- c) **(6 pts)** One of the designers at your company (who didn't take EE141) comes to you one day and says that he never understood the logic for multipliers, and proposes to build a multiplier out of a ROM instead of out of full-add and half-add cells. How large of a ROM would you need to implement a 5-bit by 3-bit multiplier? (You can quote your answer in terms of the number of rows and number of columns this ROM would need to contain.) Do you think this a good idea? Why or why not?