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6:00-7:30pm

EECS 141: FALL 2002—MIDTERM 2

For all problems, you can assume the following transistor parameters (unless mentioned otherwise):

NMOS:

$$V_{Tn} = 0.4, k'_n = 115 \mu\text{A}/\text{V}^2, V_{DSAT} = 0.6\text{V}, \lambda = 0, \gamma = 0.4 \text{ V}^{1/2}, 2\Phi_F = -0.6\text{V}$$

PMOS:

$$V_{Tp} = -0.4\text{V}, k'_p = 30 \mu\text{A}/\text{V}^2, V_{DSAT} = -1\text{V}, \lambda = 0, \gamma = -0.4 \text{ V}^{1/2}, 2\Phi_F = 0.6\text{V}$$

NAME	Last	First
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GRAD/UNDERGRAD	
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Problem 1: ____/16

Problem 2: ____/12

Problem 3: ____/10

Problem 4: ____/ 6

Total: ____/44

PROBLEM 1. Logic Styles (16pts)

In this problem, for single-ended logic styles, assume that only true inputs are available, and for differential logic styles you can use both true and complementary inputs. Draw a gate implementing $Y = AB + CD$ in:

a) Standard complementary CMOS.

b) Domino logic.

c) Dual-rail domino.

d) Transmission-gate logic (differential logic style)

PROBLEM 2. Logical effort. (12pts)

- a) (4pts) Find the logical effort for a domino buffer from the figure. Assume that the static inverter PMOS/NMOS ratio is appropriately skewed.

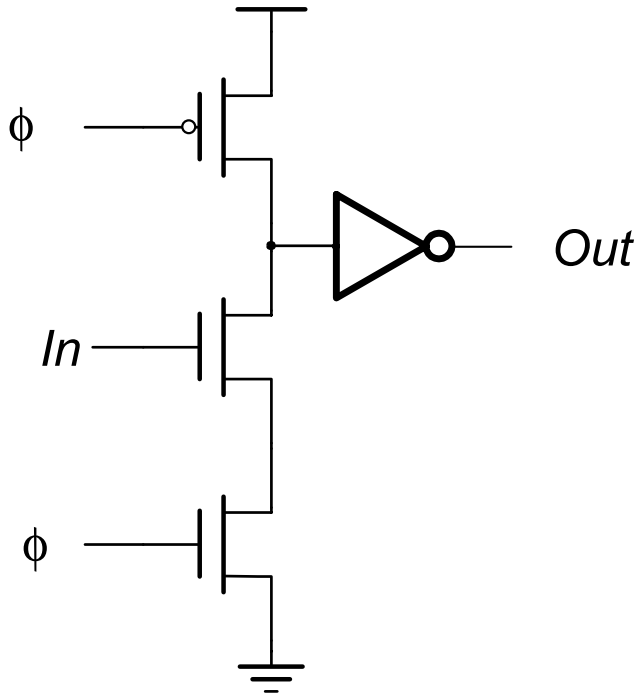


Fig. 1.

$g =$

b) (8pts) Calculate the optimal stage effort (product of the logical effort and fanout) for the domino buffer with a foot switch (as one shown in Fig.1).

(Hint: we calculated that the optimal effort for the static complementary CMOS stage is about 4. Recalculate this for the domino buffer that consists of a dynamic inverter and a skewed static inverter).

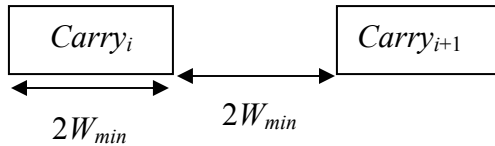
Optimal fanout =

PROBLEM 3: Arithmetic Circuits (10pts)

Consider an implementation of a bit-sliced 32-bit carry-lookahead adder implemented in static CMOS. The bit slice is 18 metal pitch, and the metal pitch is 1 μ m. You can assume that the resistance of all metal layers is 0.1 Ω/\square . The table below shows the dependence of the intra-layer capacitance per unit length for the metal layer that is used for implementation of this carry wire.

Spacing	Min	1.5 * Min	2 * Min	2.5* Min	3 * Min or more
Capacitance	80aF/ μ m	60aF/ μ m	50aF/ μ m	45aF/ μ m	40aF/ μ m

- a) (2pts) How many bit slices does the longest carry wire cross in radix-2 implementation?
- b) (2pts) How many bit slices does the longest carry wire cross in radix-4 implementation?
- c) (2pts) What is the worst-case coupling capacitance of the wire when all the carries are routed vertically with double-width, double-spaced pitch?

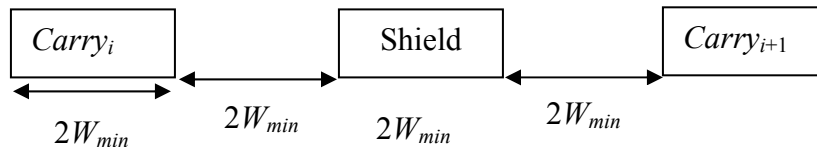


$C_{total} =$

- d) (2pts) How does this capacitance change if the wire pitch is doubled from the previous case, without changing the wire width?

$C_{total} =$

- e) (2pts) If the shielding wires are introduced in the same layer as shown before, what is the worst-case coupling capacitance?



$C_{total} =$

PROBLEM 4. Power dissipation (6 pts).

Compute the probability of the energy consuming transitions of the output, F of the logic function $F = \overline{A + B \cdot C}$, implemented in standard static CMOS, if the input probabilities are $p(A=1) = 0.2$, $p(B=1) = 0.5$, $p(C=1) = 0.1$.