

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS 130
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Midterm II - Solutions

Name: _____

SID: _____

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Total		100

Problem 1 [20pts]

Answer the following questions concisely:

In a forward-biased P⁺N diode,

- (a) [5pts] Which type of carrier (electron or hole) dominates the carrier injection across the P-N junction?

Hole.

- (b) [5pts] Which type of carrier contributes most of the stored minority carriers?

Hole.

- (c) [5pts] Which recombination lifetime (that of the N side or the P side) determines the switching speed of this diode?

N side

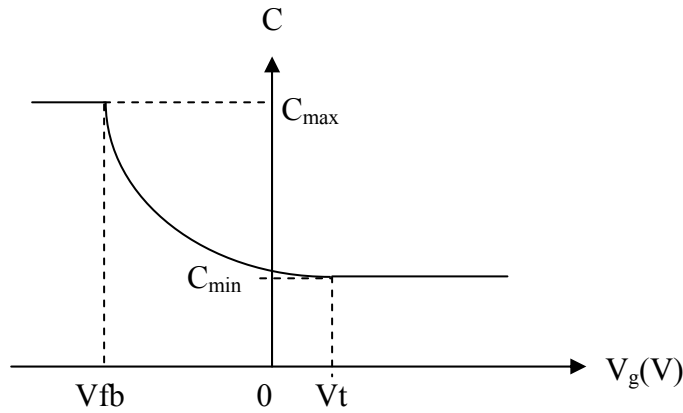
- (d) [5pts] Which side has the larger depletion region?

N side

Problem 2 [20pts]

Consider a MOS capacitor with N+ polysilicon gate and $N_a = 5 \times 10^{17} \text{ cm}^{-3}$

- (a) [10pts] The C-V characteristic of this MOS capacitor is shown below. Suppose this MOS capacitor is used in a voltage-controlled oscillator, which requires a capacitance tuning range of $\frac{C_{\max}}{C_{\min}} = 1.5$, what's the required oxide thickness (T_{ox})? Ignore poly depletion effects and inversion charge thickness effects.



$$C_{dep} = \frac{\epsilon_s}{W_{dep,max}} = 2.12 \times 10^{-7} \text{ F/cm}^2 \quad \phi_B = \frac{kT}{q} \ln \left(\frac{N_A}{n_i} \right) = 0.46V$$

$$W_{dep,max} = \sqrt{\frac{2\epsilon_s 2\phi_B}{qN_a}} = \sqrt{\frac{2 \cdot 11.7 \cdot 8.854 \times 10^{-14} \text{ F/cm} \cdot 2 \cdot 0.46V}{1.6 \times 10^{-19} \text{ C} \cdot 5 \times 10^{17} \text{ cm}^{-3}}} = 4.88 \times 10^{-6} \text{ cm} = 48.8 \text{ nm}$$

$$C_{\min} = \frac{C_{dep} C_{ox}}{C_{dep} + C_{ox}} \quad C_{\max} = C_{ox}$$

$$1.5 = \frac{C_{\max}}{C_{\min}} = \frac{C_{dep} + C_{ox}}{C_{dep}} = 1 + \frac{C_{ox}}{C_{dep}}$$

$$C_{ox} = 0.5 C_{dep} = 1.06 \times 10^{-7} \text{ F/cm}^2$$

$$T_{ox} = \frac{3.9 \cdot 8.854 \times 10^{-14} \text{ F/cm}}{1.06 \times 10^{-7} \text{ F/cm}^2} = 3.26 \times 10^{-6} \text{ cm} = 32.6 \text{ nm}$$

- (b) [5pts] Assume the fixed oxide charge density at the p-type silicon / SiO₂ interface is $N_{it} = 10^{12} \text{ cm}^{-2}$. The charge is positive. What is the flatband voltage, V_{fb} ? Assume $T_{ox} = 10 \text{ nm}$. Don't use the T_{ox} calculated in (a).

$$C_{ox} = \frac{\epsilon_{ox}}{T_{ox}} = 3.45 \times 10^{-7} \text{ F/cm}^2$$

$$\frac{qN_{ox}}{C_{ox}} = \frac{1.6 \times 10^{-19} \text{ C} \cdot 10^{12} \text{ 1/cm}^2}{3.45 \times 10^{-7} \text{ F/cm}^2} = 0.46 \text{ V}$$

$$V_{fb} = \Phi_g - \Phi_s - \frac{Q_{ox}}{C_{ox}} = -0.56 \text{ V} - 0.026 \text{ V} \cdot \ln \frac{5 \times 10^{17}}{10^{10}} - \frac{Q_{ox}}{C_{ox}} = -1.02 - \frac{qN_{ox}}{C_{ox}} = -1.48$$

- (c) [5pts] Assume there are 3 electron traps (electron states), A, B, and C in the SiO₂, as shown below. A is 0.5eV above E_f ; B is located at E_f ; C is 0.5eV below E_f . What is the probability that

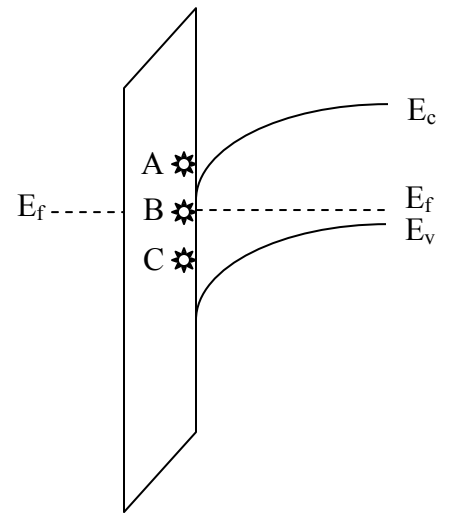
- (1) A is filled
- (2) B is empty
- (3) C is empty

$$f(E_A) = \frac{1}{1 + \exp\left(\frac{E_A - E_f}{kT}\right)} = \frac{1}{1 + \exp\left(\frac{500 \text{ meV}}{26 \text{ meV}}\right)} = 4.45 \times 10^{-9}$$

$$f(E_B) = 1 - \frac{1}{1 + \exp\left(\frac{E_B - E_f}{kT}\right)} = 1 - \frac{1}{1 + \exp(0)} = 0.5$$

$$f(E_{T,C}) = 1 - \frac{1}{1 + \exp\left(\frac{E_{T,C} - E_f}{kT}\right)} = \frac{\exp\left(\frac{E_{T,C} - E_f}{kT}\right)}{1 + \exp\left(\frac{E_{T,C} - E_f}{kT}\right)}$$

$$= \frac{4.45 \times 10^{-9}}{1 + 4.45 \times 10^{-9}} = 4.45 \times 10^{-9}$$



Problem 3 [20pts]

An n-channel MOSFET is fabricated on a p-type silicon wafer with $N_a = 10^{17} \text{ cm}^{-3}$. The gate is N+ polysilicon. $V_t - V_{fb} = 1.2\text{V}$, $\mu_{ns} = 300 \text{ cm}^2 / \text{V} \cdot \text{s}$, $T = 300\text{K}$, $m = 1$.

(a) [5pts] What is the flatband voltage, V_{fb} ?

$$V_{fb} = \psi_g - \psi_s = -\frac{E_g}{2q} - \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right) = -0.56 - 0.026 \cdot \ln\left(\frac{10^{17}}{10^{10}}\right) = -0.98$$

(b) [5pts] If a gate dielectric with a large dielectric constant (high- κ dielectric), $\epsilon_{ox} / \epsilon_0 = 25$ is used as the gate dielectric, what is the required oxide thickness (T_{ox}) to achieve $V_t - V_{fb} = 1.2\text{V}$?

$$\phi_B = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right) = 0.026 \cdot \ln\left(\frac{10^{17}}{10^{10}}\right) = 0.42$$

$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{2\epsilon_s q N_a} 2\phi_B}{C_{ox}}$$

$$C_{ox} = \frac{\sqrt{2\epsilon_s q N_a} 2\phi_B}{V_t - V_{fb} - 2\phi_B}$$

$$= \frac{\sqrt{2 \cdot 11.7 \cdot 8.8542 \times 10^{-14} \text{ F/cm} \cdot 1.6 \times 10^{-19} \text{ C} \cdot 10^{17} \text{ cm}^{-3} \cdot 2 \cdot 0.42}}{1.2 - 2 \cdot 0.42} = 4.64 \times 10^{-7} \text{ F/cm}^2$$

$$T_{ox} = \frac{\epsilon_{ox}}{C_{ox}} = \frac{25 \cdot 8.8542 \times 10^{-14} \text{ F/cm}}{4.64 \times 10^{-7} \text{ F/cm}^2} = 4.77 \times 10^{-6} \text{ cm} = 47.7 \text{ nm}$$

(c) [5pts] If $V_{gs} - V_t = 1.0\text{V}$, $V_{ds} = 1.5\text{V}$, is the transistor operating in linear region or saturation region?

$$V_{dsat} = \frac{V_{gs} - V_t}{m} = 1.0 < V_{gs} - V_t$$

The transistor is operating in the saturation region

Problem 4. [20pts]

Consider an n-channel MOSFET with a P^+ polysilicon gate, a width to length ratio of $W/L = 2$, an oxide thickness of $T_{oxe} = 10nm$, and body doping of $N_a = 5 \times 10^{16} cm^{-3}$.

[5pts] (a) Calculate the threshold voltage V_t .

$$\phi_B = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right) = 0.401 V$$

Since the gate is P^+ polysilicon gate the flat-band voltage is,

$$V_{fb} = \psi_g - \psi_s = \left(\chi_{Si} + \frac{E_g}{q}\right) - \left(\chi_{Si} + \frac{E_g}{2q} + \phi_B\right) = \frac{E_g}{2q} - \phi_B = 0.159 V$$

$$\therefore V_t = V_{fb} + 2\phi_B + \frac{\sqrt{2\varepsilon_{Si}qN_a2\phi_B}}{C_{ox}} = 0.159 + 0.802 + 0.334 = 1.295 V$$

[5pts] (b) Calculate the body-effect factor m .

$$m = 1 + \frac{3t_{ox}}{W_{dmax}} = 1 + \frac{3t_{ox}}{\sqrt{\frac{2\varepsilon_{Si}2\phi_B}{qN_a}}} = 1.208$$

[5pts] (c) Find the drain current I_D at $V_{gs} = 3.5V$ and $V_{ds} = 2V$. Use the values obtained from (a) and (b). Assume $\mu_{ns} = 250\text{cm}^2/V \cdot \text{sec}$. (If you haven't solved (a) and (b), use $V_t = 1V$ and $m = 1.3$.)

Using results from (a) and (b),

$$V_{dsat} = \frac{V_{gs} - V_t}{m} = \frac{3.5V - 1.295V}{1.208} = 1.825V < V_{ds} = 2V$$

So the transistor is in saturation.

$$\therefore I_D = \frac{W}{2mL} \mu_{ns} C_{ox} (V_{gs} - V_t)^2 = 0.348 \text{ mA}$$

Using the given values,

$$V_{dsat} = \frac{V_{gs} - V_t}{m} = \frac{3.5V - 1V}{1.3} = 1.923V < V_{ds} = 2V$$

$$\therefore I_D = \frac{W}{2mL} \mu_{ns} C_{ox} (V_{gs} - V_t)^2 = 0.415 \text{ mA}$$

[5pts] (d) Determine threshold voltage V_t with a body to source reverse bias of $V_{sb} = 2V$. Assume a constant maximum depletion width of $W_{dmax} = 0.15\mu\text{m}$ with a retrograde doping profile.

$$\begin{aligned} V_t &= V_{t0} + \alpha V_{sb} = V_{t0} + \frac{3t_{ox}}{W_{dmax}} V_{sb} \\ &= 1.295V + \frac{3 \times (10 \times 10^{-7} \text{ cm})}{0.15 \times 10^{-4} \text{ cm}} \times 2V \\ &= 1.295V + 0.2 \times 2V \\ &= 1.295V + 0.4V \\ &= 1.695V \end{aligned}$$

Problem 5. [20pts]

Design an n-channel MOSFET with a polysilicon gate to have a threshold voltage of $V_t = 1V$. Assume an oxide thickness of $T_{oxe} = 10nm$, a channel length of $L = 1\mu m$, and a body-effect factor of $m = 1$.

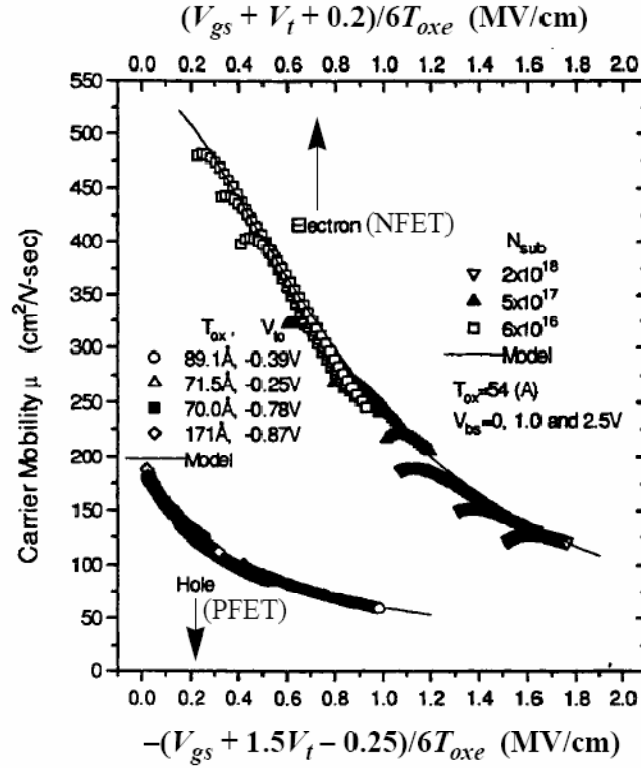
[5pts] (a) What is the standard polysilicon gate doping type for this transistor?

The standard polysilicon gate doping is N^+ .

[5pts] (c) Determine is the body doping N_a . Assume $\phi_B = 0.45V$ but do not determine N_a from $\phi_B = (kT/q)\ln(N_a/n_i)$.

$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{2\varepsilon_{si}qN_a2\phi_B}}{C_{ox}} = -\left(\frac{E_g}{2q} + \phi_B\right) + 2\phi_B + \frac{\sqrt{4\varepsilon_{si}qN_a\phi_B}}{C_{ox}}$$
$$\therefore N_a = \left(V_t + \frac{E_g}{2q} - \phi_B\right)^2 \frac{C_{ox}^2}{4\varepsilon_{si}q\phi_B} = 4.924 \times 10^{17} \text{ cm}^{-3}$$

[10pts](c) A drain current of $I_D = 1.35\text{mA}$ is required at $V_{gs} = V_{ds} = 3\text{V}$. Calculate the required device width W . Use the universal mobility curve given below to find μ_{ns} .



First we find the mobility.

$$\mathcal{E}_{eff} = \frac{V_{gs} + V_t + 0.2V}{6t_{ox}} = \frac{3V + 1V + 0.2V}{6 \times (10 \times 10^{-7}\text{cm})} = 0.7 \text{ MV/cm}$$

$$\therefore \mu_{ns} = 325 \text{ cm}^2/\text{V} \cdot \text{sec}$$

Calculating V_{dsat} show the transistor is in saturation.

$$V_{dsat} = \frac{V_{gs} - V_t}{m} = \frac{3V - 1V}{1} = 2V < V_{ds} = 3V$$

So the current is written as,

$$I_D = \frac{W}{2mL} \mu_{ns} C_{ox} (V_{gs} - V_t)^2 = 1.35 \text{ mA}$$

$$\therefore W = \frac{2 \cdot m \cdot L \cdot I_D}{\mu_{ns} C_{ox} (V_{gs} - V_t)^2} = 6.015 \text{ } \mu\text{m}$$