UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

FINAL EXAMINATION
EE 130/230M: IC Devices, Fall 2012
Time allotted: 75 minutes

NAME: ______________________ ______________________

STUDENT ID#: __________________

INSTRUCTIONS:

1. **Unless otherwise stated, assume**
   a. **temperature is 300 K**
   b. **material is Si**

2. **SHOW YOUR WORK. (Make your methods clear to the grader!)**
   Specially, while using chart, make sure that you indicate how you have got your numbers. For example, if reading off mobility, clearly write down what doping density that corresponds to.
3. **Clearly mark (underline or box) your answers.**
4. **Specify the units on answers whenever appropriate.**

SCORE: 1	__________	**/ 20**
2	__________	**/ 20**
3	__________	**/ 20**
Total	__________	**/ 60**

PHYSICAL CONSTANTS

Description	Symbol	Value
Electronic charge	q	1.6×10^{-19} C
Boltzmann's constant	k	8.62×10^{-5} eV/K
Thermal voltage at 300K	$V_T = kT/q$	0.026 V

PROPERTIES OF SILICON AT 300K

Description	Symbol	Value
Band gap energy	E_G	1.12 eV
Intrinsic carrier concentration	n_i	10^{10} cm^{-3}
Dielectric permittivity	ε_{Si}	1.0×10^{-12} F/cm

USEFUL NUMBERS

$V_T\ln(10) = 0.060$ V at T=300K
$\exp(0.6/0.26)\sim10^{10}$

Depletion region Width: $W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)\left(V_{bi}-V_{Applied}\right)}$

Law of the Junction: $np = n_i^2\left(e^{qV_D/kT}\right)$

$N_c=2.8\times10^{19}/cm^3$

$N_V=1.04\times10^{19}/cm^3$

Prob 1. [20 pts]

(a) [4 pts] Answer the following

(i) [2 pts] What are the main physical mechanisms for drift and diffusion?

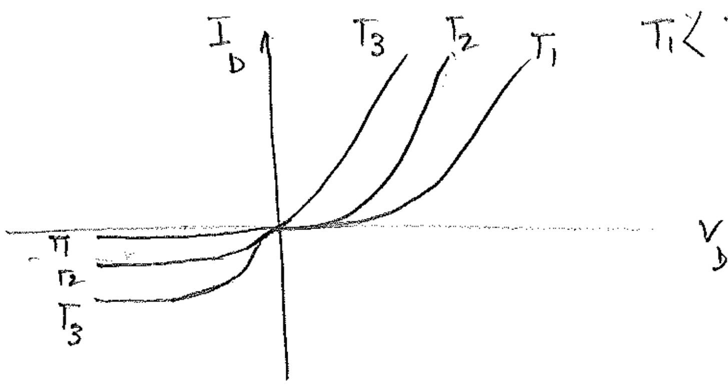
Drift → acceleration due to electric field

Diffusion → random thermal motion

(ii) [2 pts] Between two diodes, one more heavily doped than the other, which one will have a smaller reverse breakdown voltage? Why?

The heavily doped one. Due to high doping, built in E-field will be high and large band overlap will occur at even relatively small reverse bias. This will lead to tunneling and then breakdown.

(b) [5 pts] Drawing an I-V plot show how ***increasing temperature from 300˚K*** **will change the current voltage characteristic of a diode. You should show three different I-Vs each for a different temperature. In the plots carefully show if there is any difference in the extent of change in current for forward and reverse bias. Briefly justify reasons for any such difference.**



$T_1 < T_2 < T_3$

Forward bias:

$$I \propto e^{-\frac{E_g}{kT}} e^{\frac{qV_D}{kT}}$$

$$\propto e^{\left(\frac{qV_D - E_g}{kT}\right)}$$

Reverse bias:

$$I \propto e^{-E_g/kT}$$

Diode range of operation for low level injection $|qV_D| < E_g$

At same $|V_D|$ increase in forward bias current is less than reverse bias current.

(c) [5 pts] Consider a pn junction diode doped such that $N_A=10^{17}/cm^3$ and $N_D=10^{15}/cm^3$. A bias is applied such that at the edge of the depletion region on the p-side the number of electrons is found to be $10^8/cm^3$. Is the diode forward or reverse biased? Justify your answer. Also find out the amplitude of the bias voltage applied across the diode.

$n_p = 10^8$; $n_{p_0} = \frac{10^{20}}{10^{17}} = 10^3$. $n_p > n_{p_0} \rightarrow$ forward biased

$$\delta n_p = \frac{n_i^2}{N_A} \left(e^{\frac{qV_D}{kT}} \right)$$

$$\Rightarrow 10^8 = \frac{10^{20}}{10^{17}} e^{\frac{V_D}{0.026}}$$

$$\Rightarrow 10^5 = e^{\frac{V_D}{0.026}}$$

$$V_D = 0.026 \ln 10^5 = 0.06 \times 5 = 0.3V$$

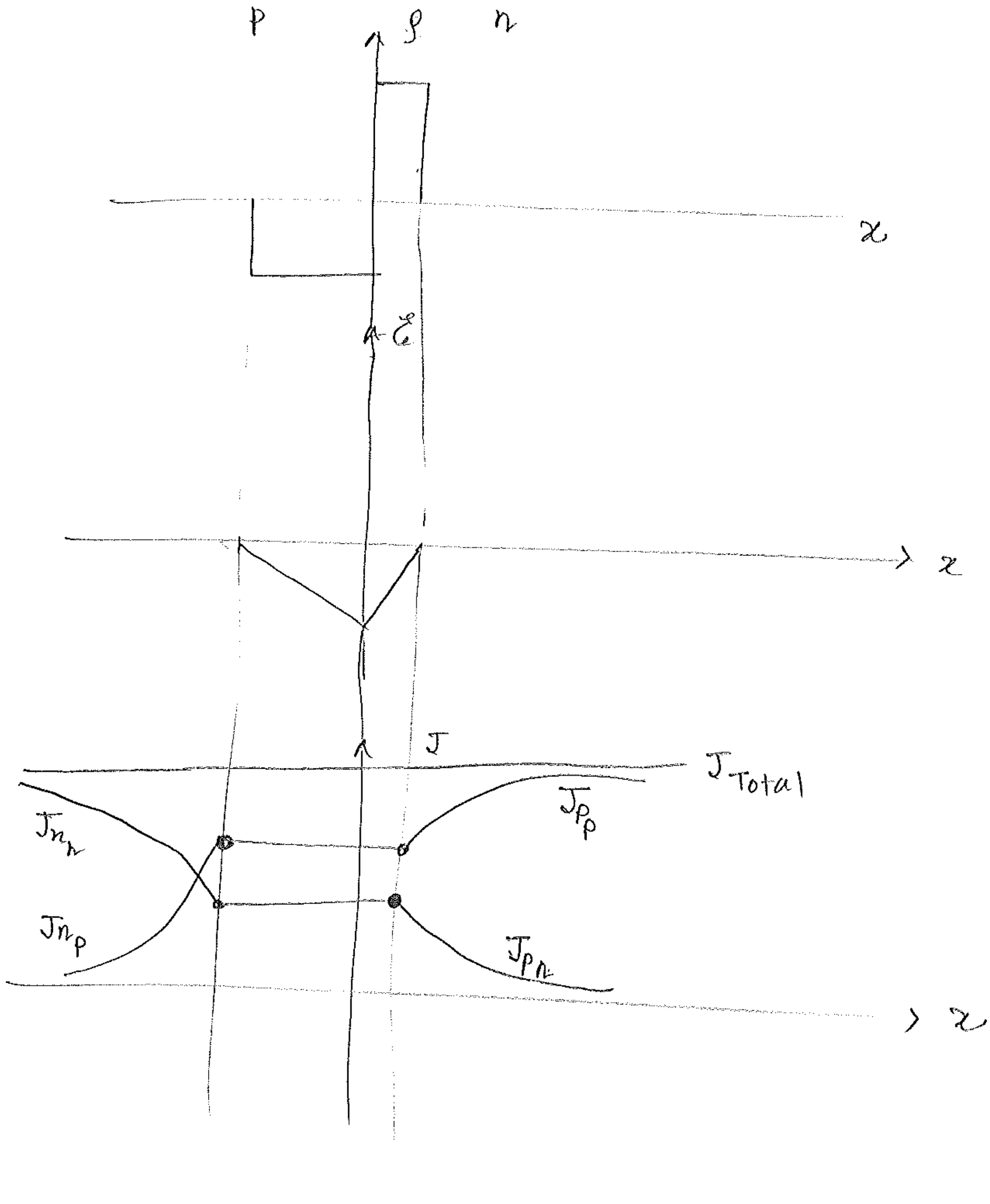
$$\boxed{V_D = 0.30\ V}$$

(d)[6 pts] Consider a pn junction diode is biased such that the n-side has a higher doping than the p-side. Qualitatively draw:

(i) The charge density profile

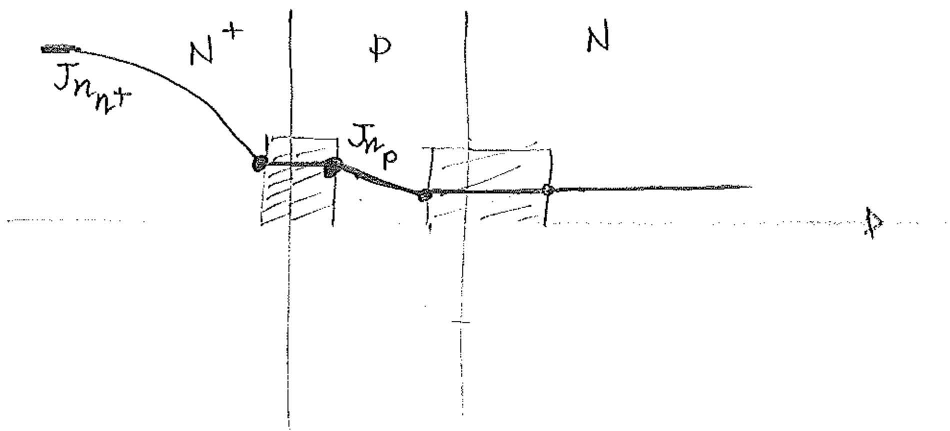
(ii) The electric field profile

(iii) The current density profile in the forward bias



Prob 2 [20 pts]

(a) [5 pts] Consider a short base $N^{+}PN$ junction. Draw the current density profile due to electrons in the various regions of the junction in the forward active mode. Comment on how it will change if the base width is increased. In both cases, assume that emitter and collector regions are much longer than diffusion lengths.



The amplitude of collector current density will decrease with increasing base width because more and more carriers will be lost in the base due to recombination.

(b) [9 pts] Two pnp BJTs are designed such that:

T1: $N_{E1}>N_{B1}>N_{C1}$

T2: $N_{c2}>N_{B2}>N_{E2}$

In both cases, the base doping is the same $N_{B1}=N_{B2}$. Also, $N_{E1}=N_{C2}$.

(a) Which transistor is expected to have greater emitter efficiency? Explain.

(b) Which transistor will exhibit greater sensitivity to base width modulation under active mode biasing? Explain.

(c) Which transistor will breakdown at smaller voltages? Explain.

(a) T1: more carriers will be injected from emitter than from base

(b) T2: Because base will get a larger depletion region

(c) T2: B-C Junction has higher doping.

(c)[6 pts]

(i) [3 pts] How will changing the base width affect the speed of a bipolar transistor?

increasing base width will increase the strrage time.

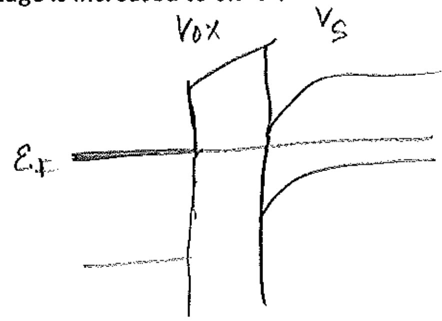
(ii) [3 pts] $\beta=I_C/I_B$ falls down at very high and low levels of collector current. What are the reasons for that?

high currents → high level injection

low currents → junction leakage.

Prob 3[20 pts]

(a) [8 pts] Consider a MOS capacitor with N+ polysilicon gate that has a doping of N_D=2.8 x 10^{19}/cm^3. Assume the applied gate voltage is 0.5 V and a body doping of N_A= 10^{17}/cm^3. Find out the voltage drop across the gate oxide if it is known that, at this gate voltage, the depletion region width in the body is 110 nm. What will be the voltage drop across oxide if the gate voltage is increased to 0.7 V ?



$$V_{fb} = -kT \ln \frac{2.8\times10^{19}\times10^{17}}{10^{20}} = -0.98\ eV$$

$$\phi_B = kT \ln \frac{10^{17}}{10^{10}} = 0.42\ eV$$

$$V_g = V_{fb} + V_{ox} + V_s$$

$$W = 110\times10^{-7} = \sqrt{\frac{2\varepsilon}{qN_A} V_s}$$

$$\therefore V_s = \frac{qN_A W^2}{2\varepsilon} = 0.923\ V$$

$$\therefore V_{ox} = V_g - V_{fb} - V_s = +0.5 - (-0.98) - 0.923$$

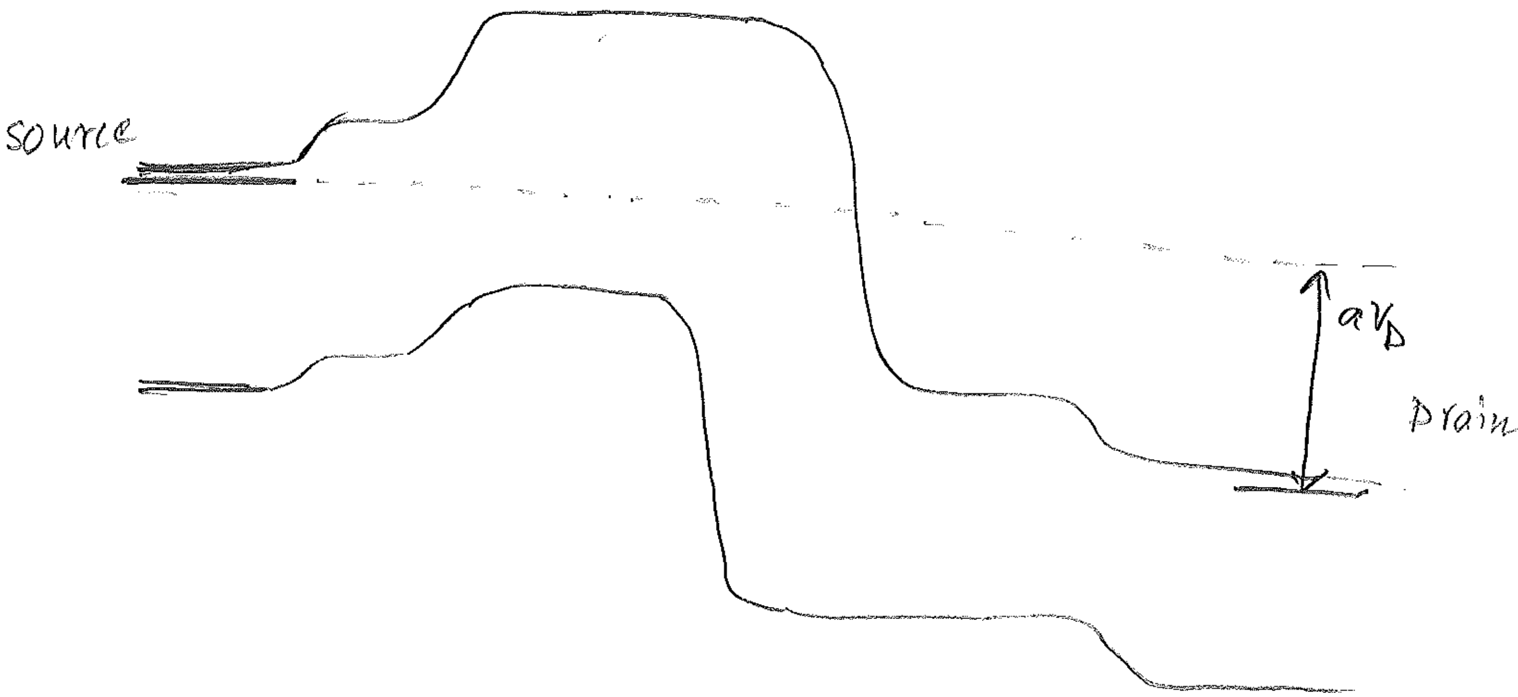
$$\boxed{V_{ox} = 0.5561\ V}$$

We note: $V_s > 2\phi_B$; thus the MOSFET is in inversion. Therefore any increase in gate voltage drops across oxide.

Hence when $V_g = 0.7$ V

$$\boxed{V_{ox} \cong 0.55 + 0.2 \simeq 0.75\ V}$$

(b) [6 pts] Consider a N+NPNN+ Junction made on a p-type substrate. The N+ regions are connected to metal as source and drain. This structure is topped with a thin SiO_2 and a metal gate. Draw the energy band diagram *at the interface between semiconductor and the SiO_2* going from source to drain at the OFF condition. How do you think the inclusion of extra N+ regions will affect the MOSFET performance?



Extra N+ reduces source resistance.

(c) [6 pts]

(i) [3 pts] Briefly explain DIBL.

lowering of the potential barrier at the source by drain voltage in very small MOSFET is called DIBL. Due to close proximity of drain terminal, drain voltage modulates the channel potential which in a long channel FET is only controlled by gate.

(ii) [3 pts] Si has bandgap of 1.1 eV while InAs has a bandgap of ~0.3 eV . For an ultra scaled transistor, which material will give the most leakage current? Why? Assume that the current due to direct tunneling through gate insulator is the same for both.

InAs → increased BTBT due to small gap.

→ increased n_i^2 → increased reverse saturation current