(Note: Greek letters are in caps, "micro" is represented by a 'u'.)

Default bipolar transistor parameters:

\[ n_{pn}: \beta = 100, V_a = 50 \text{ V}, V_{BE,oh} = 0.7 \text{ V}, V_{CE,sat} = 0.2 \text{ V}, V_{th} = 25 \text{ mV}. \]

Default MOS transistor parameters: note that LAMBDA depends on L!

\[ u_{n}C_{ox} = 50 \text{ uAV}^{-2}, \Lambda = [0.1/L] \text{ V}^{-1} (L \text{ in } \mu\text{m}), V_{Tn} = 1 \text{ V}, C_{ox} = 2 \text{ fF/um}^{2}, C_{in} = 0.1fF/um^{2}, C_{JSWn} \]

\[ u_{p}C_{ox} = 50 \text{ uAV}^{-2}, \Lambda = [0.1/L] \text{ V}^{-1} (L \text{ in } \mu\text{m}), V_{Tp} = -1 \text{ V}, C_{ox} = 2 \text{ fF/um}^{2}, C_{jp} = 0.1fF/um^{2}, C_{JSWp} \]

**Problem #1 : Bipolar Transresistance Amplifier [20 points]**

Given:

\[ ISUP_1 = 200\mu\text{A}; R_{OC1} = 750k\Omega \]
\[ V_{SUP1}, \text{min} = 0.15\text{V}, 0.45\text{V} \]

\[ ISUP_1 = 100\mu\text{A}; R_{OC2} = 200k\Omega \]
\[ V_{SUP2}, \text{min} = 0.3\text{V} \]

\[ I_{BIAS} = -200\mu\text{A}, V_{OUT} = 0\text{V} \]

(a) [2 pts.] Identify the stages of this two-stage transresistance amplifier by labeling the two-ports below with "CE", "CB", or "CC" for common-emitter, common-base, or common-collector. Also, label node "X".

(b) [3 pts.] Find the numerical value of the small-signal input resistance of this amplifier, \( R_{in} \).
*Your answer need only be correct to within (+/-)5% for full credit.*

(c) [3 pts.] Find the numerical value of the small-signal output resistance of this amplifier, \( R_{out} \).
*Your answer need only be correct to within (+/-)5% for full credit.*

(d) [5 pts.] Find the numerical value of the "two-port" transresistance \( R_{m} \) of this amplifier (with \( R_s = \infty \) and \( R_L = \infty \)).
*Your answer need only be correct to within (+/-)5% for full credit.*
(e) [3 pts.] Find the numerical value of $v_{out}/s$ for $R_s = 500$ OMEGA and $R_t = 10$ kOMEGA. If you couldn't solve parts (b)-(d), you can assume without loss of credit that $R_{in} = 2.2$ kOMEGA, $R_{out} = 4$ kOMEGA, $R_m = -185$ kOMEGA. Needless to say, these are not the correct answers to (b)-(d).

(f) [2 pts.] Find the numerical value of the minimum output voltage $V_{OUT, min}$ of this amplifier.

(g) [2 pts.] Find the numerical value of the maximum output $V_{OUT, max}$ of this amplifier.

Problem #2 : CMOS Digital Logic Gate [20 pts.]
(a) [5 pts.] Draw the schematic for this Logic gate, including the (W/L)'s of the transistors in (um/um). Substrate and well contacts are omitted for this simplified layout; you can consider that the "select" mask is the same as the "n well" mask.

(b) [2 pts.] Write the logic function implemented by this logic gate. If you couldn't do part (a), you can use the following circuit.

(c) [4 pts.] Find the numerical value of $C_{db}$ for this logic gate in fF. You should identify clearly which areas on the layout contribute to $C_{db}$, and you don't need to have done part (a) in order to answer this part; useful device information is located on the cover page of the exam.

(d) [3 pts.] Find the numerical value of $C_w$ for this logic gate in fF. Note that you don't need to have done part (a) in order to answer this part. The wiring capacitance per unit area is $C_w = 0.1 fF/\text{um}^2$.

(e) [2 pts.] Find the numerical value of $C_s$ for this logic gate in fF. Note that you don't need to have done part (a) in order to answer this part.

(f) [2 pts.] What is the worst-case charging current for the load capacitance $C_l$ for this amplifier in uA? If you couldn't do part (a), you can use the substitute logic gate given in part (b).

(g) [2 pts.] What is the worst-case discharging current for $C_l$ of this amplifier in uA? If you couldn't do part (a), you can use the substitute logic gate given in part (b).

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**Problem #3 : Current Sources [10 points]**
(a) [4 pts.] Using exactly 4 transistors, draw the circuit schematic of a CMOS current source that will implement $i_{SUP}$ (sourcing current from the positive supply), using $I_{REF}$ as a reference.

(b) [3 pts.] Given: $I_{REF} = 25 \text{ uA}$ and $I_{SUP} = 75 \text{ uA}$. If all except one of the transistors have widths $W = 10 \text{ um}$ and all of the transistors have lengths $L = 2 \text{ um}$, find the width of the remaining transistor. There may be more than one correct answer to this part.

(c) [3 pts.] Find the maximum voltage $V_{OUT, max}$ for which this current supply will have all of its transistors in operating the constant-current region. If you were unable to solve (b), assume that the width of the PMOS current-source output transistor is $W = 100 \text{ um}$.