Problem #1
BiCMOS Transresistance Amplifier [22 points]

(a) [4 pts.] Draw the two-port small-signal model for this two-stage amplifier, with the small-signal source (and R_S) and the load resistor R_L attached. Your model should show the cascaded models for each stage; there is no need to substitute the expressions for the input and output resistances and gain elements for each stage.

(b) [4 pts.] Find the numerical value of the input resistance of this amplifier, R_in.

(c) [4 pts.] Find the numerical value of the output resistance of this amplifier, R_out. Your answer need only be correct to within plus or minus 5% for full credit.

(d) [6 pts.] Find the numerical value of the transresistance R_m. Note that R_S = infinity and R_L = infinity for calculating this two-port parameter. Your answer need only be correct to within plus or minus 5% for full credit.

(e) [4 pts.] If the current supplies I_BIAS, i_SUP,1, and i_SUP,2 all need a minimum voltage of 0.5 V across
them in order to function, what are the maximum and minimum values of \( v_{\text{OUT}} \)? (In other words, find the output swing of the transresistance amplifier.)

**Problem #2**
Static CMOS Logic Gate [18 points]

(a) [5 pts.] What is the logic operation performed by the above circuit? In other words, what is the logical expression for \( Q \) in terms of the three inputs, \( A \), \( B \), and \( C \)? Note: you can use a truth table to answer this question.

(b) [4 pts.] We would like to have the worst case low-to-high and high-to-low propagation delays to be equal. Find the required relationship between the width-to-length ratio \((W/L)_n\) of the NMOS transistor and the width-to-length ratio \((W/L)_p\) of the PMOS transistors.

(c) [5 pts.] This logic gate has no load capacitance or wire capacitance (it does have parasitic drain-to-bulk capacitances, however.) Find the channel length transistors \( L_p = L_n \) so that the worst case low-to-high propagation delay \( t_{\text{PLH}} = 10^{-11} \text{s} = 100 \text{ps} \).

Given: \( MU_p = 100 \text{ cm}^2/\text{Vs} \), \( C_{\text{ox}} = 2.5 \text{ fF/um}^2 \), and the drain-to-bulk capacitance of each transistor is \( C_{\text{DB}} = (1/3) C_{\text{ox}} W L \).

If you couldn't solve part (b), you can assume that \((W/L)_p = 2.5(W/L)_n\) for this part (not the correct answer to (b), of course.)

(d) [4 pts.] Find the ratio of the best case propagation delays.

\[
t_{\text{PHL}}/t_{\text{PLH}}
\]

If you couldn't solve (b), you can assume that \((W/L)_p = 2.5 (W/L)_n\) for this part (not the correct answer to (b), of course.)
Problem #3
Bipolar Transistor Physics [10 points]

Given:

\[ N_{dE} = 10^{18} \text{cm}^{-3}, \]
\[ N_{aB} = 5 \times 10^{16} \text{cm}^{-3}, \]
\[ N_{dC} = 4 \times 10^{15} \text{cm}^{-3}. \]

The base and emitter widths are \( W_B = W_E = 0.25 \text{ um} \). The area of the emitter-base junction is \( A_E = 1000 \text{ um}^2 \) and the area of the base-collector junction is \( A_C = 3000 \text{ um}^2 \). The electron diffusion coefficient in the base is \( D_{nB} = 10 \text{cm}^2/\text{s} \) and the hole diffusion coefficient in the emitter is \( D_{pE} = 5 \text{cm}^2/\text{s} \). The charge on an electron is \( q = 1.6 \times 10^{-19} \text{C} \).

(a) [5 pts.] For the bias condition where \( V_{\text{OUT}} = 2.5V \), sketch the minority carrier concentration in the base on the graph below. Label the numerical value of \( n_pB \) (\( x = 0 \)).

(b) [5 pts.] Find the numerical value for the bias voltage \( V_{\text{BIAS}} \) for which the bipolar transistor just enters saturation (\( V_{\text{OUT}} = 0.2V \)).

Solutions!

Posted by HKN (Electrical Engineering and Computer Science Honor Society)
University of California at Berkeley
If you have any questions about these online exams please contact examfile@hkn.eecs.berkeley.edu.