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EECS 105, Spring/1992
Final Examination
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- Default bipolar transistor parameters:
  npn: !!1! data
- Default MoOS transistor parameters:
  NMOS: !!!! data
  PMOS: !!!! data

Problem #1 Device Physics[20 points]

Given: Rather than the default parameters on the cover sheet, the above bipolar transistor has the following properties:

Current gain: !!!(Bata)=100
Base-collector capacitance: !!!!(data), where the collector-base voltage is in volts
Base transit time: !!!(data)
The capacitors C1,C2, and !!!(CE) and all blocking capacitors.

(a) [4 points] Find the numerical value of !!!() for the DX operating point defined in the circuit above.

(b) [4 points] The cross section of the transistor at the operating point found in part(a) is shown below. The base-emitter depletion width is one-fourth the base-collector deplention width. Find the numerical value of !!!() for the circut above.

(c) [4 points] Find the numerical value of the Miller capacitor !!(CM) for this inverting amplifier, along with the numerical value of its comer(-3 dB) frequency,fc.

(d) [4 points] The circuit is modified by reducing the voltage supply to the collector from 6V to 3V, as shown in the schematic below. Note that the voltage supply to the base is left unchanged. What is the numerical value of !!!()? Accurately sketch the new base-collector depletion width on the cross section.

(e) [4 point] For the modified circuit in part (d), find the numerical value of the Miller capacitor !!!(CM), along with the numerical value of its comer(-3 dB) frequency,fc.

Problem #2. Differential Amplifier [20 point]

(a) [4 point] What is the numerical value of the DC collector current in Q1? You cna use the average value of the two input voltages to find Ic1.

(b) [4 point] What is the small-signal differential half-circuit for this amplifier? What is the numerical value of the differential gain, ad?

(c) [4 point] What is the small-signal common-mode half-circuit for this amplifier? What is the numerical value of the common-mode gain, ac?

(d) [4 point] What is the numerical value of the *total* output voltage, !!(vo1)? *Note*: the error band is *not* 10% for this part -- use both the bias and small-signal models to arrive at your answer.

(e) [4 point] What is the numerical value of the *total* output voltage, !!(vo2)? *Note*: the error band is *not* 10% for this part -- use both the bias and small-signal models to arrive at your answer.

Problem #3. Single-ended Amplifier with Active Load [20 point]

(a) [4 points] What are the collector currents in all transistors? Verify that all are forward active, assuming that Vo=2V.

(b) [4 points] What are the maximum and minimum values of the output voltage, V., such that all transistors are forward active?

(c) [4 points] What is the numerical value of the input resistance, Ri?

(d) [4 points] What is the numerical value of the output resistance, Ro?

(e) [4 points] What is the numerical value of the small-signal voltage gain,Vo/Vs?

Problem #4."NMOS with PMOS load" Logic Gate [20 point]

(W/L) is given next to each transistor label; use the default NMOS and PMOS parameters. for each device, the body is shorted to the source (connection not shown).

(a) [4 points] What is the numerical value of the drain current !!!(data) of device M2? *Hint:* both M1 and M2 are diode-connected and have identical geometries.

(b) [4 points] For the case where VB = 0 V, plot the load line of device ML on the output characteristices of device MA, which are given below.

(c) [4 points] Plot the out put voltage Vo as a function of the input voltage VA on the graph below. You can

use the answer part(b) (hint: the easy way) or derive analytical expressions. Label the operating regions of transistors MA and ML on the transfer curve.

(d) [4 points] What logical function is implemented by this logic gate? Show with a truth table. Consider 0V to correspond to logic "0" and 5V to correspond to logic "1".

(e) [4 points] It is desirable to reduce the supply voltage to say 3V from 5V. As a result, the threshold voltage of the NMOS devices should be reduced (and the magnitude of the PMOS threshold reduced, as well). In the floolowing table, label the dirction of change of the parameters in order to decrease the threshold voltage. The parameters are: !!(data) the oxidee thickness, !!(data) the permittivity of the oxide (which can be changed be using a different insulating thin film), NA the substrate doping, and Tg the gate polysilicon thickness. If the parameter doesn't affect the threshold voltage, use a "-" in the table.

!!!!!!!! Need a TABLE

Problem #5. Bipolar operational amplifier [20 point]

The op amp above uses "super !!(Bata)" transistors Q1 and Q2 in the differential input stage. The properties of these transistors are:
!!!data
All other transistors have the default properties which are given on the cover page of the exam.

Hints: this three-stage op amp has two differential gain stages and is biased by three current sources -- all of them referenced to the same resistor.

(a) [2 points] Find the DC collector currents in all transistors and verify that alll are forwardactive. You can assume that the two inputs and the output are at DC ground for biasing.

(b) [4 points] Find the maximum and the minimum DC common-mode input voltages, !!!data adn !!!data for which all transistors remain in the forward-active region. In case you were unable to solve part (a), you can assume that the collector currects for *all* transistors is 100!!!data -- which is incorrect, of course.

(c) [2 points] Find the numerical value of the differential input resistance, Rid.

(d) [3 points] Find the two-port model for the fifferential input stage, where the small-signal input voltage is V1-V2 and the output voltage is !!!data. Note: you'll need to find the numerical values of the differential output resistance of the input stage, !!!data and ists differential transconductance, !!data. (Use the value of !!data from part(c)). Draw the circuit model!

(e) [3 points] Find the two-port model for the second stage of the op amp, where the small-signal input voltage is !!!data and the small-signal output voltage is !!data. Draw the circuit modle and find the numerical values!

(f) [3 points] Find the numerical value of the small-signal differential votage gain of the op amp,by using your small-signal two-port models ofr the first two stages and adding the model for the third stage. The differential voltage gain is defined as:
!!!! data

(g) [3 points] Find the -3 dB frequency for this op amp. You can neglect the contribution of !!data in your calculations.