University of California at Berkeley
College of Engineering
Department of Electrical Engineering
and Computer Sciences

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EECS 105
Midterm 2: November 19, 1997

· Closed book and notes; one 8.5" X 11 "formula sheet (both sides)
· Do all work on exam pages
· You have 80 minutes; use your time wisely!
· Default BJT parameters:

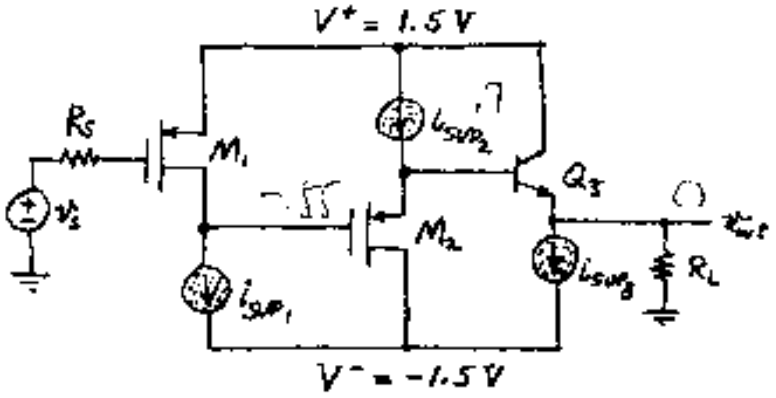
npn: $B_o = 100$, $V_{An} = 0.7$ V, $V_{CE,sat} = 0.2$ V

· Default MOSFET parameters: note that λ depends on L!

NMOS: $\bullet_n C_{ox} = 50\ \bullet AV^{-2}$, $\lambda_n = [0.1/L]V^{-1}$ (Lin •m) $V_{Tn} = 1$ V

PMOS: $\bullet_p C_{ox} = 25\ \bullet AV^{-2}$, $\lambda_p = [0.1/L]V^{-1}$ (Lin •m) $V_{Tp} = -1$ V

1. BiCMOS Voltage Amplifier [19 points]



GIVEN:
$V_{SG_2} = 1.25$V
$L_1 = L_2 = 2\mu m$; $W_2 = 256\mu m$
$R_S = R_L = 10\,k\Omega$
$I_{SUP_1} = 250\mu A$ $r_{oc_1} = 80\,k\Omega$
$I_{SUP_2} = 100\mu A$ $r_{oc_2} = 200\,k\Omega$
$I_{SUP_3} = 100\mu A$ $r_{oc_3} = 200\,k\Omega$

(a) [3 pts.] What is the numerical value of the DC voltage V_{G2} at the stage of the transistor M_2, given that the DC output voltage $V_{out} = 0$ V? Note that V_{SG2} is given.

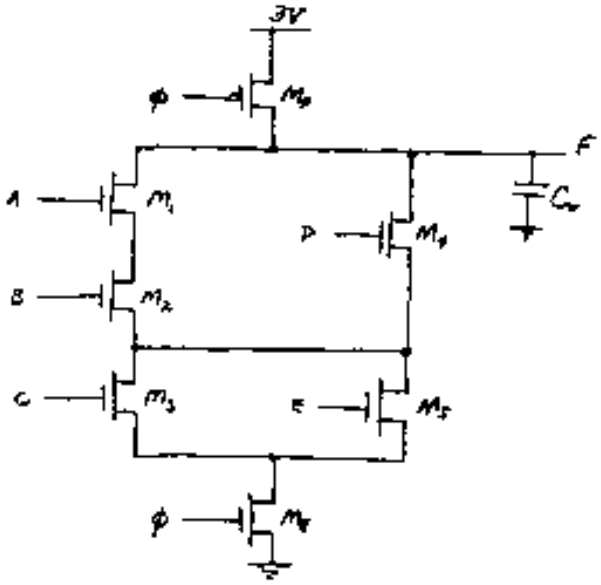
(b) [3 pts.] Find the width of the transistor M_1 in •m such that $-I_{D1} = I_{SUP1} = 250$ •A, with M_1 operating in the constant-current region (MOSFET saturation). Neglect channel-length modulation for this DC Hand-calculation.

(c) [3 pts.] Draw the two port models for each stage of this three stage voltage amplifier. You do not need to evaluate parameters of the models.

(d) [5 pts.] Find the numerical value of the output resistance R_{out} of this amplifier. *Your answer need only be correct to within ±5% for full credit.*

(e) [5 pts.] Find the numerical value of the voltage gain A_v ($R_s = 0\ \Omega$, $R_L = \infty\ \Omega$). If you If you couldn't answer part (b), you can assume for this part that $W_1 = 100$ •m. *Your answer need only be correct to within ±5% for full credit.*

2. Dynamic Logic Gate [15 points]



Given:

$W = 4\ \mu m$
$L = 2\ \mu m$
$L_{diff} = 4\ \mu m$
} ALL MOSFETS

$C_J = 2\ fF/\mu m^2$
WIRE CAPACITANCE / LENGTH = $1.6\ fF/\mu m$

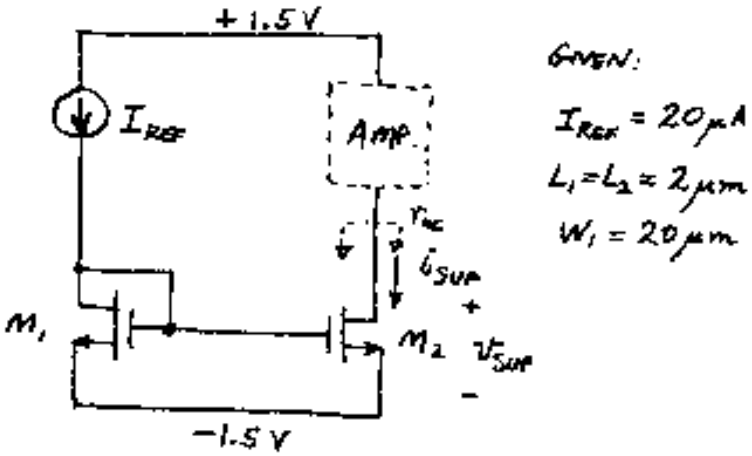
(a) [4 pts.] With a fanout of zero (no gates coneected to the output F), the load capacitance is equal to the parasitic capacitance. Find the numerical value of the parasitics capacitance C,sub>p for the case where a 50 •m-long wire is attached to F. Identify (by circling them), those transistors that contribuate to the drain-bulk capacitance C_{DB}.

(b) [4 pts.] Find the numerical value of the precharge t_{PLH} of this dunamic logic gate. If you couldn't solve part (a), you can assume that $C_p = C_L = 100$ fF for this part.

(c) [4 pts.] Find the numerical value of the worst case evaluation time t_{PHL} of this dynamic logic gate. If you couldn't solve part (a), you can assume that $C_p = C_L = 100$ fF for this part

(d) [3 pts.] Find a logical expression F in terms of the inputs A, B, C, D, and E. There is no need to simplify the expression.

3. MOSFET Current Source [16 points]



(a) [3 pts.] In the above schematic, the dotted box contains the amplifier towhich the current supply is attached. We want the DC supply to be $I_{SUP} = 50$ •A. What is the required width of transistor M_2 in •m?

(b) [3 pts.] Find the numerical value of the small-signal source resistance r_{oc} of this current source. Note that r_{oc} is indicated on the schematic.

(c) [3 pts.] Find the numerical value of the gate voltage V_{G2} of transistor M_2.

(d) [4 pts.] Plot i_{sup} vs v_{sup} characteristics on the axes below. Your values for $V_{sup,min}$ and I_{sup} should be numerically accurate. There is no need to include channel-length modulation effects on your plot.

(e) [3 pts.] We would like to obtain a source resistance of 2 MΩ. Find the width and length of transistor M_2 needed to achieve this goal without changing I_{sup}