## EECS 105, Fall 1992 <br> Final Exam <br> Professor R. T. Howe

- Closed book; three 8\&\#189" x 11" crib sheets (both sides)
- Do all work on exam pages.
- Default bipolar transistor parameters:
npn: $\& \# 223_{\mathrm{n}}=100, v_{A n}=100 \mathrm{~V}, c_{\mathrm{PIH}}=15 \mathrm{pF}, c_{\& \# 18}=1 \mathrm{pF}$.
pnp: $\& \# 223_{\mathrm{p}}=50, v_{A p}=50 \mathrm{~V}, c_{[\mathrm{PI]}]}=30 \mathrm{pF}, c_{\& \# 181}=2 \mathrm{pF}$.
- Default MOS transistor parâmeters:

NMOS: \&\#181 $C^{\prime}=25 \& \# 181 \mathrm{AV}^{-2}$, , LAMBDA $_{\mathrm{n}}=0.01 \mathrm{~V}^{-1}, v_{T_{n}}=1 \mathrm{~V}$. PMOS: \&\#181 ${ }_{p}^{n} c_{o x}^{, o x}=10 \& \# 181 \mathrm{AV}^{-2}$, [LAMBDA $]_{\mathrm{p}}^{n}=0.02 \mathrm{~V}^{-1}, v_{T p}^{T n}=-1 \mathrm{~V}$.

## Problem \#1 (Single-ended BJT amplifier) [20 points] Picture of a circuit should be here!

## Problem \#1a [3 points]

Find the numerical value of the following resistors:
$R_{E 1}, R_{\text {REF }}, R_{E 3}$
such that the DC input voltage $V_{I}$, the DC output voltage $V_{O}$ are both zero, and all bias currents are 100 \&\#181A.

## Problem \#1b [3 points]

Find the numerical value of the input resistance $R_{i}$ of this amplifier. Use

## $R_{E 1}=5 \mathbf{k}[\mathrm{OHM}] \mathrm{s}$

if you couldn't do part (a)--not the correct answer for part (a), of course.

## Problem \#1c [4 points]

Find the numerical value of the output resistance $R_{o}$ of this amplifier. Use

## $R_{E 3}=10 \mathrm{k}[\mathrm{OHM}] \mathrm{s}$

if you couldn't do part (a)--not the correct answer for part (a), of course.

## Problem \#1d [3 points]

Draw the 2-port small-signal model for this three stage amplifier. Label all input and output resistances and controlled sources.

## Problem \#1e [4 points]

What is the numerical value of the small-signal voltage gain, $v_{o} / v_{i}$ ?

## Problem \#1f [3 points]

What is the maximum value the output voltage can reach and still have all devices operating in the forward active region?

## Problem \#2 (Electrostatics in Thermal Equilibrium) [18 points] Picture of an $n^{+}-p-n$ layer and 2 graphs should be here!

Given: the above $n^{+}-p-n$ is in thermal equilibrium. The donor and acceptor doping concentrations are shown below the structure. You can assume that the $n^{+-} p$ depletion layer has a total width of $0.5 \& \# 181 \mathrm{~m}$ and that the $p-n$ depletion layer is $1 \& \# 181 \mathrm{~m}$ wide in your sketches.

## Problem \#2a [6 points]

Sketch the electrostatic potential $[\mathrm{sPHI}](x)$ along the $x$ axis on the graph below; your values in the bulk regions (outside the depletion layers) should be accurate.

## Problem \#2b [6 points]

Sketch the electric field $E(x)$ along the $x$ axis on the graph below. Your field values should be accurate in the bulk regions (hint: this shouldn't be too hard if you recall the definition of bulk silicon!) and qualitatively correct in the depletion regions.

## Problem \#2c [6 points]

Plot (note: must be accurate!) the charge density, normalized by the electron charge, on the log plot below. Hint: recall that the depletion layer widths are given, along with the doping concentrations.

## Problem \#3 (Frequency Response) [16 points] Picture of a circuit should be here!

## Problem \#3a [3 points]

Redraw the schematic with the transistor current sources replaced current-source symbols and find numerical values for the source/sink currents.

## Problem \#3b [4 points]

Find the numerical value of the voltage gain $A_{\nu}=v_{o} / v_{s}$.

## Problem \#3c [5 points]

Find the numerical value of the corner frequency of this amplifier, $f_{c}$. Note that the transistor capacitances are given on the first page.

## Problem \#3d [4 points]

Given: the amplifier has a second pole at 6.4 MHz . Plot the magnitude of the amplifier voltage gain in dB as a function of frequency on the graph below.

## Problem \#4 ("Interesting" BiMOS Logic Gate) [14 points] Picture of a circuit should be here!

$(W / L)=5$. Other transistor parameters are given on the first page.

## Problem \#4a [2 points]

Plot the load characteristic $i_{L}$ as a function of $v_{O}$ for the npn transistor on the graph below.

## Problem \#4b [4 points]

Plot the driver characteristics $\left|i_{D}\right|$ on the same graph below, for $v_{I}=0,1,2,3,4$, and 5 V .

## Problem \#4c [4 points]

From your results in part (b), plot the transfer curve $v_{O}$ as a function of $v_{I}$ on the graph below.

## Problem \#4d [4 points]

Label the operating regions for the p-channel MOSFET and for the npn BJT on the transfer curve. You need not find the exact breakpoints between the different segments, but the labels should be qualitatively correct.

## Problem \#5 (Two-stage differential amplifier) [20 points] Picture of a circuit should be here!

## Problem \#5a [3 points]

Draw the 2-port small signal model for this op amp as a cascade of the two differential amplifiers. You need not evaluate all of the parameters in this part.

## Problem \#5b [3 points]

Find the numerical value for the transconductance of the first stage,
$G_{m 1}$

## Problem \#5c [4 points]

Find the numerical value for the transconductance of the second stage,
$G_{m 2}$

## Problem \#5d [3 points]

Find the numerical value of the differential input resistance of the second stage,

## $R_{i d 2}$

## Problem \#5e [4 points]

Find the numerical value of the output resistance of the amplifier $R_{o}$.

## Problem \#5f [3 points]

Given that the two small-signal input voltage waveforms are:
$v_{i 1}=(-5 \& \# 181 \mathrm{~V}) \cos ([s O M E G A] t)$ and
$v_{i 2}=(-8.5 \& \# 181 \mathrm{~V}) \cos ([\mathrm{sOMEGA}])$.
Find the output waveform $v_{o}(t)$. You can assume that [sOMEGA] is much less than the corner frequency of the differential amplifier.

## Problem \#6 (npn BJT and n-channel MOSFET Operating Regions) [12 points] <br> Problem \#6a [6 points]

The plots below show the minority carrier concentrations in the emitter, base, and collector for six operating points, labeled $A-F$ on the ouput characteristics. Fill in the table by correctly identifying which cross section corresponds with which operating point.

## Picture of a bode plot, 6 cross sections and matching boxes should be here!

## Problem \#6b [6 points]

The device structures below show (qualitatively) the mobile electron charge | $Q_{n}(y) \mid$ in the channel of the MOSFET, along with the dotted outline of the edge of the depletion layer formed with the p-type substrate. Fill in the table by correctly identifying which device structure corresponds with which operating point $A-F$ on the drain characteristics.

## Picture of a bode plot, 6 device structures and matching boxes should be here!

> Posted by HKN (Electrical Engineering and Computer Science Honor Society) University of California at Berkeley If you have any questions about these online exams please contact examfile@hkn.eecs.berkeley.edu.

