UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 105: Microelectronic Devices and Circuits

MIDTERM EXAMINATION #2
Time allotted: 80 minutes

NAME: Solutions
(print) Last First Signature

STUDENT ID#: _______________________

INSTRUCTIONS:
1. Use the values of physical constants provided below.
2. SHOW YOUR WORK. (Make your methods clear to the grader!)
3. Clearly mark (underline or box) your answers.
4. Specify the units on answers whenever appropriate.

<table>
<thead>
<tr>
<th>PHYSICAL CONSTANTS</th>
<th>PROPERTIES OF SILICON AT 300K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>Symbol</td>
</tr>
<tr>
<td>Electronic charge</td>
<td>q</td>
</tr>
<tr>
<td>Boltzmann’s constant</td>
<td>k</td>
</tr>
<tr>
<td>Thermal voltage at 300K</td>
<td>V_T =</td>
</tr>
<tr>
<td></td>
<td>kT/q</td>
</tr>
</tbody>
</table>

Note that V_T ln(10) = 0.060 V at T=300K

SCORE:

1 ________ / 15

2 ________ / 15

3 ________ / 20

4 ________ / 15

5 ________ / 15

Total: ________ / 80
**Problem 1 [15 points]: Cascodes**

a) What is the advantage of using a BJT ($Q_2$, as shown below on the left) rather than a resistor ($R_{E}$, as shown below on the right) to achieve a high value of output resistance ($R_{out}$)? [3 pts]

$Q_2$ provides a large degeneration resistance ($\approx R_{D2}$) without sustaining a large voltage drop ($V_{EC2}$) as compared with $R_{E}$ for which the voltage drop $V_{E} \approx I_c R_{E}$ can be large if $R_{E}$ is large. Thus, the use of a BJT rather than a resistor provides for larger headroom for the output voltage signal to swing.

b) Suppose a PNP cascode is to be used as a 0.1mA current source, as shown below. What should be the values of the bias voltages $V_{b1}$ and $V_{b2}$? Assume that $I_b = 10^{-16}$A for each BJT, and that the $Q_2$ collector junction is forward-biased by no more than 0.3V to ensure that $Q_2$ operates in active mode. $V_{CC} = 2.5V$. Note that $e^{0.72} 0.026 \approx 10^{12}$ [8 pts]

In order for $I_c = I_{c2} = 0.1 mA = 10^{-4} A$,

$|V_{BE}|$ for each BJT should be $V_T \ln \left( \frac{I_c}{I_s} \right)$:

$|V_{BE}| = 0.026 \ln \left( \frac{10^{-4}}{10^{-16}} \right) = 0.026 \ln 10^{12} = 12 \times 0.060 = 0.72V$

$V_{b2} = V_{CC} - V_{EB2} = 2.5V - 0.72V = 1.78V$

If the $Q_2$ collector junction is forward-biased by 0.3V,

$V_X - V_{b2} = 0.3V \Rightarrow V_X = V_{b2} + 0.3V = 1.78V + 0.3V = 2.08V$

$c)$ Suppose that a PNP cascode is to be used as a voltage amplifier, as shown below. Which transistor ($Q_1$ or $Q_2$) should be used as the amplifying device? Explain briefly. [4 pts]

$Q_2$ should be used as the amplifying transistor.

If the input voltage signal is applied to the base of $Q_1$, the voltage gain is not as high, due to emitter degeneration.
Problem 2 [15 points]: Current Mirrors
Consider the circuit shown below:

a) What is the purpose of the transistor $Q_{REF}$? [2 pts]

$Q_{REF}$ generates a bias voltage for the base of the current-mirror transistor $Q_1$.

b) Derive an expression for $I_{copy}$ in terms of $I_{REF}$ and $m$, neglecting the effect of the transistor base currents. [3 pts]

Assuming that $I_{C,REF} = I_{REF}$, $V_X = V_T \ln \left( \frac{I_{REF}}{I_{S,REF}} \right) = V_T \ln \left( \frac{I_{copy}}{I_{S,1}} \right)$

$\Rightarrow \frac{I_{REF}}{I_{S,REF}} = \frac{I_{copy}}{I_{S,1}} \Rightarrow I_{copy} = \frac{I_{S,1}}{I_{S,REF}} I_{copy}$

$\frac{I_{S,1}}{I_{S,REF}} = \frac{mA_E}{A_E} = m$

$\Rightarrow I_{copy} = mI_{REF}$

c) Considering the effect of the transistor base currents, what is the error in $I_{copy}$? [8 pts]

$Q_{REF}$ base current is $\frac{I_{C,REF}}{\beta} = \frac{I_{copy}}{m\beta}$

$Q_1$ base current is $\frac{I_{copy}}{\beta}$

Applying KCL: $I_{REF} = I_{C,REF} + \frac{I_{C,REF}}{\beta} + \frac{I_{copy}}{\beta} = \frac{I_{copy}}{m} + \frac{I_{copy}}{m\beta} + \frac{I_{copy}}{\beta}$

$I_{REF} = \frac{I_{copy}}{m} \left[ 1 + \frac{1}{m} + \frac{1}{\beta} \right] = \frac{I_{copy}}{m} \left[ 1 + \frac{1}{\beta} + \frac{m}{\beta} \right]$

$I_{copy} = mI_{REF} \left[ 1 + \frac{m+1}{\beta} \right] = mI_{REF} \left( 1 - \frac{m+1}{\beta} \right)$

$\Rightarrow$ fractional error is $-\frac{m+1}{\beta}$

d) How can the error in $I_{copy}$ be reduced, without changing $I_{REF}$? [2 pts]

The error in $I_{copy}$ can be reduced by using another transistor to supply the base currents for $Q_{REF}$ and $Q_1$:

In this case, the fractional error is reduced by the factor $\beta$, since $I_{B,REF} = \frac{1}{\beta} (I_{B,REF} + I_{B,1})$. 
Problem 3 [20 points]: Frequency Response
Consider the amplifier stage shown below. Assume that \( V_A \neq \infty \) for \( Q_1 \) and \( Q_2 \).

![Amplifier Stage Diagram]

a) Write an expression for the low-frequency voltage gain. [4 pts]

This is a common-emitter stage with \( "R_C" = R_{o1} \parallel R_{o2} \):

\[
A_V = -g_mZ\left(\frac{1}{R_{o1}} \parallel \frac{1}{R_{o2}}\right)
\]

b) Why is the voltage gain of this amplifier dependent on the signal frequency? [2 pts]

The BJTs have junction capacitances, whose impedances depend on the signal frequency.

c) Draw the BJT junction capacitances \( (C_{\mu 1}, C_{\mu 2}, C_{CS1}, C_{CS2}, C_{\mu 1}, C_{CS2}) \) on the circuit diagram above. [6 pts]

d) Use Miller’s theorem to derive an expression for the bandwidth. Assume that the dominant pole is associated with the input node. [6 pts]

The floating capacitance \( C_{\mu 2} \) can be converted into a grounded capacitance at the input node \( C_{\mu 2}(1-A_V) \).

The total capacitance seen at the input node is \( C_{\pi 2} + C_{\mu 2}(1-A_V) \).

The resistance seen at the input node is \( R_{\pi 2} \).

The pole associated with the input node is \( \omega_{p, in} = \frac{1}{R_{\pi 2}\left[C_{\pi 2} + C_{\mu 2}(1-A_V)\right]} \)

which is the bandwidth (in units of rad/s)

e) Considering your answers to parts (a) and (d) above, describe the trade-off between voltage gain and bandwidth. [2 pts]

In order to achieve large voltage gain, \( g_{m2} \) should be large.

If \( g_{m2} \) is large, then \( R_{\pi 2} = \frac{B}{g_{m2}} \) is small \( \Rightarrow \) bandwidth will be large.

\( \Rightarrow \) There is no trade-off between \( A_V \) and \( BW. \) (Actually, \( \omega_{p, in} \) will not be the dominant pole anymore.)
Problem 4 [15 points]: MOSFETs

a) Consider a long-channel MOSFET with the $I-V$ characteristic as shown below.

i) What is the threshold voltage ($V_{TH}$) of this device? [2 pts]

From the plot, $V_{DSAT} = 0.5 \text{V}$.

$V_{DSAT} = V_{GS} - V_{TH} \Rightarrow V_{TH} = V_{GS} - V_{DSAT} = 0.5 \text{V}$

ii) Indicate (by drawing a dashed curve on the plot) how the $I-V$ characteristic would change if $V_{GS} - V_{TH}$ were to be decreased by a factor of 2. [3 pts]

$V_{DSAT}$ decreases by $2X$

$I_{DSAT} = (V_{GS} - V_{TH})^{2}$ decreases by $4X$

$\lambda$ is unchanged

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b) Indicate how the small-signal parameters of a long-channel MOSFET would change, if the gate-oxide thickness were to be decreased. Assume $V_{GS} - V_{TH}$ remains the same. Give qualitative explanations for your answers. [6 pts]

<table>
<thead>
<tr>
<th>MOSFET Parameter</th>
<th>Parameter will (check one)</th>
<th>Brief Justification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transconductance, $g_m$</td>
<td>√</td>
<td>Capacitive coupling of the channel potential to the gate voltage is increased, so $V_G$ will have a stronger influence on $I_D$</td>
</tr>
<tr>
<td>Output resistance, $r_o$</td>
<td>√</td>
<td>The channel-length modulation effect is not affected by $t_{OX}$, i.e., $\lambda$ does not change. However, $I_D$ increases if $t_{OX}$ increases (for the same reason as above) and so $r_o = \frac{1}{\lambda I_D}$ decreases.</td>
</tr>
</tbody>
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e) What is the channel length modulation effect? [2 pts]

The drain current increases with increasing $V_{DS}$ in the saturation region of operation, due to the length of the inversion-layer channel decreasing.

e) Why does the drain current eventually saturate in a short-channel MOSFET, as the drain-to-source voltage ($V_{DS}$) is increased? [2 pts]

The drain current in a short-channel MOSFET eventually saturates as $V_{DS}$ increases, due to velocity saturation.
Problem 5 [15 points]: MOSFET Amplifiers

Consider the MOSFET amplifier stage shown below. Assume that $\lambda \neq 0$ for each of the long-channel MOSFETs.

a) What type of amplifier is this [2 pts]? Circle one of the following, and justify your answer:

- [ ] Common Emitter
- [ ] Common Base
- [ ] Follower
- [ ] Cascode

Input signal is applied to _gate_ of $M_2$.
Output signal is taken from _drain_ of $M_2$.

b) What is the purpose of transistor $M_3$? [2 pts]

$M_3$ serves as a current source.

c) What is the purpose of the capacitor $C_1$? [2 pts]

$C_1$ is used to couple the input voltage signal to the _gate_ of the amplifying transistor ($M_2$), without affecting the DC bias.

d) Derive expressions for the low-frequency voltage gain ($A_v$), input resistance ($R_{in}$), and output resistance ($R_{out}$). [9 pts]

The resistance seen looking into the drain of $M_2$ is approximately

$$g_{m2}r_{o2} \cdot \left( \frac{1}{g_{m1} || r_{oi}} \right)$$

so the total resistance seen looking into the output node is

$$R_{out} = r_{o3} || g_{m2}r_{o2} \cdot \left( \frac{1}{g_{m1} || r_{oi}} \right) \approx r_{o3} || r_{o2} \quad \text{since} \quad g_{m1} \approx g_{m2} \quad \text{(since} \quad I_{D1} = I_{D2})$$

Since the resistance looking into the gate of $M_2$ is infinite,

$$R_{in} = R_1 || R_2$$

$$A_v \approx \frac{R_1 || R_2}{R_c + R_1 || R_2} \cdot \frac{-r_{o3}}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$