Problem 1 [20 points]: Semiconductor Basics
Consider a Si pn junction diode, maintained at $T = 300K$, with a structure and potential distribution as shown.

a) Estimate the resistivity of the more lightly doped side. [5 pts]

\[ n = N_D = 10^{16} \text{ cm}^{-3} \]
\[ \mu_n = 1200 \text{ cm}^2/\text{V.s} \]
\[ q\mu_n n_i = 1.6 \times 10^{-19} \times 1200 \times 10^{16} = 2 \]
\[ \rho = \frac{1}{q\mu_n n_i} = \frac{1}{2} \frac{J}{\text{cm}} \]

b) Calculate the built-in potential, $V_0$. [4 pts]

\[ V_0 = \frac{kT}{q} \ln \left( \frac{N_A N_D}{n_i^2} \right) = 0.026 \ln \left( \frac{10^{19} \times 10^{16}}{10^{20}} \right) = 0.026 \ln 10^{15} \]
\[ = 15 \times (0.026 \ln 10) = 15 \times 0.60 \text{ mV} = 9 \text{ mV} \]


c) What is the bias voltage, $V_B$? [3 pts]

Total potential drop across junction = $V_0 - V_D = 2 \text{ V}$
\[ => V_B = V_0 - 2 \text{ V} = -1.1 \text{ V} \]

d) Calculate the areal junction (depletion) capacitance. [3 pts]

\[ C_J = \frac{\varepsilon_s}{W_{depl}} = \frac{10^{-12} \text{ F/cm}}{0.5 \times 10^{-6} \text{ cm}} = 2 \times 10^{-8} \text{ F/cm}^2 \]

e) Show qualitatively (by sketching a curve on the plot above) the potential distribution $V(x)$ for $V_B = 0 \text{ V}$. [2 pts]

f) Why does a reverse-biased pn junction have an associated (voltage-dependent) small-signal capacitance? [3 pts]

The depletion charge changes with the bias voltage, i.e., a change in $V_B$ requires a change in $Q_{depl}$ on either side of the junction. \[ C_J = \frac{\partial V_0}{\partial Q_{depl}} \]
Problem 2 [20 points]: Bipolar Junction Transistor

a) What is the base-width modulation effect, and why is it undesirable? [4 pts]

An increase in $|I_C|$ with increasing $|V_C E|$ due to decreasing quasi-neutral base width ($W$) with increasing reverse bias on the collector junction. This results in a finite output resistance ($r_o < \infty$) which degrades the intrinsic gain of the BJT.

b) How should the base region of a BJT be designed to maximize current gain, and what is the trade-off? [4 pts]

- The base should be more lightly doped than the emitter ($N_b < N_e$)
- The quasi-neutral base width should be short ($W << L_B$)
- Trade-off is large base-width modulation effect (low $V_A$ and $r_o$)

c) Consider a BJT with the $I-V$ characteristics as shown below.

![I-V Characteristics](image)

i) Draw the small-signal model for the DC bias condition $V_{BE} = 0.8V, V_{CE} = 2.5V$. [9 pts]

(Indicate numerical values and units for the small-signal parameters, and label the transistor terminals.)

\[ I_C = 9mA \Rightarrow \beta = \frac{9mA}{80\mu A} = 112.5 \]

\[ V_T = \frac{E}{B} = \frac{112.5}{0.35} = 320V \]

\[ r_o = \frac{\partial V_{CE}}{\partial I_C} = \frac{5V}{2mA} = 2.5k\Omega \]

Small-signal model:

![Small-signal Model](image)

ii) Indicate by sketching a curve on each of the plots above, for $V_{BE} = 0.75V$, how the $I-V$ characteristics would change if the base dopant concentration were to be increased by a factor of 2. [3 pts]
Problem 3 [20 points]: BJT Amplifiers

Consider the amplifier stage as shown. Assume \( V_A = \infty \) and active mode operation for the BJT.

a) What are the purposes of \( C_1 \) and \( C_B \)? [4 pts]

- \( C_1 \) allows the input signal to be coupled to the BJT, without disturbing its DC bias point
- \( C_B \) provides an AC ground for the BJT, to increase the voltage gain.

b) Write expressions for the small-signal voltage gain (\( A_V \)), input resistance (\( R_{in} \)), and output resistance (\( R_{out} \)). [8 pts]

\[
\begin{align*}
\text{Circuit for AC analysis:} & \quad \text{This is a common-base amplifier with} \\
R_C & \quad \text{(} R_i \text{ and } R_C \text{ are in parallel between output node and AC ground.)} \\
R_1 & \quad \text{\"} R_C \text{\"} = R_C \parallel R_1 \\
R_2 & \quad \text{\"} R_B \text{\"} = 0 \\
R_3 & \quad \text{\"} R_E \text{\"} = R_S \parallel R_E \\
\end{align*}
\]

\[
A_V = \frac{R_C \parallel R_1}{\frac{1}{S_m} + R_S \parallel R_E} \quad \frac{R_E}{R_S + R_E}
\]

\[
R_{in} = R_E \parallel \frac{1}{S_m}
\]

\[
R_{out} = R_C \parallel R_1
\]

c) Describe the trade-off between headroom and voltage gain, in selecting the value for \( R_C \). How can this tradeoff be alleviated? [6 pts]

- For large headroom, \( R_C \) should be small (so that the BJT collector is biased at a voltage \( \gg V_B \)).
- For large voltage gain, \( R_C \) should be large.
- This trade-off can be alleviated by increasing \( V_{cc} \).

d) What is the main disadvantage (weakness) of this voltage amplifier design? [2 pts]

Small \( R_{in} \) (approximately \( \frac{1}{S_m} \)), undesirable in most cases except when \( R_S \) is very small.
Problem 4 [20 points]: MOSFETs

a) Explain why the current \( I_D \) in a long-channel MOSFET saturates with increasing drain-to-source voltage \( V_{DS} \). [3 pts]

As the drain voltage increases to become greater than \( V_{GS} - V_{TH} \), the inversion layer in the channel becomes pinched off at the drain end.

As \( V_D \) is increased beyond \( V_{GS} - V_{TH} \), the voltage dropped across the pinch-off region increases, while the voltage across the inversion layer remains the same. Since the lateral E-field doesn't increase with \( V_D \), \( V_D \) doesn't increase with \( V_D \).

b) How can the channel length modulation effect be minimized, and what is the trade-off? [3 pts]

The channel length modulation effect can be reduced by:
- increasing \( L \), and/or
- increasing \( N_D \) (which increases \( V_{TH} \))
to reduce the size of the pinch-off region relative to \( L \).
The trade-off is lower \( g_m \), hence lower gain.

c) Consider a MOSFET with threshold voltage \( V_{TH} = 0.5V \), biased such that \( V_{GS} = 1.0V \), with the I-V characteristic shown.

i) Is this a long-channel or short-channel MOSFET? Justify your answer. [2 pts]

\[ V_{DS(th)} = 0.25V, \text{ which is less than } V_{GS} - V_{TH} = 0.5V \]

ii) Indicate by sketching a curve on the plot how the I-V characteristic would change if \( V_{GS} \) were to be increased by 0.5 V. [3 pts]

\[ V_{GS} - V_{TH} \text{ is doubled, } \Rightarrow I_D \text{ is doubled.} \]

iii) What is the output resistance \( (r_o) \) of this MOSFET? [3 pts]

\[ r_o = \frac{\partial V_{DS}}{\partial I_D} = \frac{1V}{0.5mA} = 2 \text{ k}\Omega \]


e) Indicate in the table below how the parameters of a short-channel MOSFET would change, if the carrier mobility were to be enhanced (e.g. by 2x). Provide qualitative reasoning for your answers. [6 pts]

<table>
<thead>
<tr>
<th>MOSFET Parameter</th>
<th>Parameter will</th>
<th>Brief Justification</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>increase</td>
<td>higher ( \mu ) \rightarrow \text{higher velocity of carriers injected into the channel. }</td>
</tr>
<tr>
<td></td>
<td>decrease</td>
<td>( = ) an incremental change in # of carriers (due to ( \Delta V_{GS} ) ) \rightarrow \text{larger incremental change in } I_D</td>
</tr>
<tr>
<td></td>
<td>not change</td>
<td></td>
</tr>
<tr>
<td>Transconductance, ( g_m )</td>
<td>√</td>
<td></td>
</tr>
<tr>
<td>Output resistance, ( r_o )</td>
<td>√</td>
<td>( \Delta V_{TH} \text{ causes } V_{TH} \text{ to be reduced as } V_{GS} \text{ increases. If } \mu \text{ is increased, then the magnitude of the increase in current (} I_D \text{) with decreasing } V_{TH} \text{ is increased.} )</td>
</tr>
</tbody>
</table>
**Problem 5 [20 points]: MOSFET Amplifiers**

a) For a given bias current, why is the transconductance for a MOSFET generally smaller than that for a BJT? [4 pts]

For a BJT, \( g_m = \frac{I_c}{V_T} \). For a MOSFET, \( g_m = \frac{2I_D}{V_{GS} - V_{TH}} \).

Typically, a MOSFET requires a bias \( V_{GS} - V_{TH} \gg 2V_T \) (usually \( \approx 0.5\) V) to achieve comparable current. \( \Rightarrow g_m \) is larger for a BJT.

b) Consider the amplifier circuit below. \( M_1 \) and \( M_2 \) are long-channel MOSFETs with \( \mu_n C_{ox} = 200 \mu A/V^2 \), \( V_{TH} = 0.4V \), and \( \lambda = 0 \), and are biased such that \( I_{D1} = I_{D2} = 0.1mA \). \( V_{DD} = 1.8V \). \( W/L_1 = 16 \) and \( (W/L)_2 = 1 \).

i) What is the DC bias voltage at the input (\( V_{G1} \))? [4 pts]

\[
I_{D1} = \frac{1}{2} \left( \frac{W}{L} \right)_1 \mu_n C_{ox} (V_{GSS} - V_{TH})^2
\]
\[
(V_{GSS} - V_{TH})^2 = \frac{2I_{D1}}{\left( \frac{W}{L} \right)_1 \mu_n C_{ox}} = \frac{2 \times 10^{-4}}{16 \times 200 \times 10^{-6}} = \frac{1}{16}
\]
\[
V_{GSS} - V_{TH} = \frac{1}{4} \text{ V} = 0.25 \text{ V}
\]
\[
V_{GSS} = 0.25 \text{ V} + 0.4 \text{ V} = 0.65 \text{ V}
\]

ii) What is the voltage gain? (A numerical answer is required.) [5 pts]

This is a common source amplifier with \( "R_o" = \frac{1}{g_{m2}} \)

\[
A_v = -g_{m1} \left( \frac{1}{g_{m2}} \right)
\]
\[
g_{m} = \sqrt{2I_D \mu_n C_{ox} \left( \frac{W}{L} \right)}
\]
\[
= -\sqrt{\frac{(W/L)_1}{(W/L)_2}}
\]
\[
= -\sqrt{\frac{1}{4}} = -\frac{1}{2}
\]

iii) Calculate the headroom, i.e. the maximum amplitude of the small-signal output voltage for which \( M_1 \) operates in saturation. [7 pts]

\[
\text{Headroom} = (V_{DD} - V_{GS2}) - (V_{GSS} - V_{TH})
\]
\[
I_{D2} = \frac{1}{2} \left( \frac{W}{L} \right)_2 \mu_n C_{ox} (V_{GS2} - V_{TH})^2
\]
\[
(V_{GS2} - V_{TH})^2 = \frac{2I_{D2}}{\left( \frac{W}{L} \right)_2 \mu_n C_{ox}} = \frac{2 \times 10^{-4}}{200 \times 10^{-6}} = 1
\]
\[
V_{GS2} - V_{TH} = 1
\]
\[
V_{GS2} = 1 + V_{TH} = 1.4 \text{ V} \Rightarrow \text{headroom} = 1.8 - 1.4 - 0.25 = 0.15 \text{ V}
\]
Problem 6 [20 points]: MOSFET Cascode Stage and Current Mirror

a) Consider the cascode amplifier stage below. $M_1$ and $M_2$ are each long-channel MOSFETs, with $\lambda \neq 0$.

\[ V_{DD} \]
\[ V_{in} \]  
\[ M_2 \]
\[ V_{b1} \]  
\[ M_1 \]
\[ V_{out} \]  
\[ I_1 \]  
\[ R_{out} \]

i) What is the purpose of transistor $M_1$? [2 pts]

To boost the output impedance (and hence the gain) of this amplifier stage.

ii) Describe qualitatively how the gates should be DC biased. [4 pts]

- The gate voltage for $M_2$ should be set such that $I_{D2} = I_1$
- The gate voltage for $M_1$ should be set such that $|V_{GS1}|$ results in $I_{D1} = I_1$ and $|V_{GS2}| > |V_{GS} - V_{TH}|$

iii) Derive expressions for the voltage gain ($A_v$) and output resistance ($R_{out}$). [4 pts]

The resistance seen looking into the drain of $M_1$ is $\approx g_{m1} r_{o1} r_{o2}$

The current source is ideal, with infinite small-signal resistance.

\[ R_{out} = g_{m1} r_{o1} r_{o2} \]

\[ A_v = -g_{m2} R_{out} = -g_{m2} g_{m1} r_{o1} R_{o2} \]

b) Consider the current mirror circuit below:

\[ I_{REF} \]
\[ V_{DD} \]  
\[ M_1 \]
\[ \frac{W}{L} \]
\[ M_{REF} \]  
\[ \frac{W}{L} \]
\[ I_1 \]

i) What is the purpose of the reference transistor $M_{REF}$? [2 pts]

It generates the bias voltage needed for the mirror transistor ($M_1$) to produce a scaled copy of the reference current ($I_{REF}$).

ii) Derive an expression for $I_1$ in terms of $I_{REF}$, assuming that $\lambda = 0$. [4pts]

\[ I_D \propto \frac{W}{L} (V_{GS} - V_{TH}) \quad \Rightarrow \quad \frac{I_1}{I_{REF}} = \frac{(W/L)_1}{(W/L)_{REF}} \quad \text{since} \quad V_{GS1} - V_{TH} = V_{GS_{REF}} - V_{TH} \]

\[ \Rightarrow \quad I_1 = 2 I_{REF} \quad \text{the ideal value} \]

iii) Suppose now that $\lambda \neq 0$. If $M_1$ is operating under the condition $V_{DS} > V_{GS}$, would $I_1$ be larger or smaller than $I_{REF}$? Explain briefly. [4 pts]

$I_D$ is increased by the factor $1 + \lambda (V_{DS} - V_{DS_{REF}}) = 1 + \lambda (V_{DS} - V_{GS} + V_{TH})$

For $M_{REF}$, $V_{DS} = V_{GS}$ so this factor is $1 + \lambda V_{TH}$

For $M_1$, $V_{DS} > V_{GS}$ so this factor is $> 1 + \lambda V_{TH}$ \quad $\Rightarrow \quad I_1 > \text{ideal value}$
**Problem 7** [20 points]: Frequency Response

Consider the amplifier stage below. Assume $\lambda \neq 0, g_m r_o > 1$, and saturation mode operation for each MOSFET.

a) Write an expression for the low-frequency voltage gain from node $X$ to node $Y$, i.e. $A_{v,XY}$. [3 pts]

$$ A_{v,xy} = \frac{v_x}{v_y} = -g_{m1} \left( \frac{1}{g_{m2}} \right) \approx -1 $$

b) Write an expression for the low-frequency voltage gain of the entire stage, i.e. $A_v = v_{out}/v_{in}$. [3 pts]

$$ A_v = -g_{m1} \left( g_{m2} r_{o2} v_{o1} || R_D \right) \approx -g_{m1} R_D $$

c) Draw the MOSFET capacitances ($C_{Gd1}, C_{Gd2}, C_{SB1}, C_{DB1}, C_{Gd3}, C_{Gd2}, C_{SB2}, C_{DB2}$) on the circuit diagram above. [4 pts]

d) Use Miller's theorem to derive an approximate expression for the bandwidth. Assume that the dominant pole is associated with node $Y$, $a_{p,Y}$. [7 pts]

Using Miller's theorem, $C_{Gd1}$ contributes a grounded capacitance to node $Y$ with the value

$$ C_{Gd1} \left( 1 - \frac{1}{A_{v,xy}} \right) \approx 2 C_{Gd1} $$

The total grounded capacitance at node $Y$ is therefore

$$ C_{GB2} + C_{SB2} + C_{DB1} + 2C_{Gd1} $$

The (small-signal) resistance seen between node $Y$ and AC ground is

$$ r_{o1} || \frac{1}{g_{m2}} \approx \frac{1}{g_{m2}} $$

The dominant pole frequency (bandwidth) is thus

$$ \frac{1}{g_{m2} \left[ C_{GB2} + C_{SB2} + C_{DB1} + 2C_{Gd1} \right]} $$

e) Sketch the Bode plot on the axes provided. Label the low-frequency voltage gain and bandwidth. [3 pts]

\[ 20 \log (-g_{m1} R_D) \rightarrow \log \omega \, \text{(rad/s)} \]

\[ +20 \text{dB/dec} \]

\[ \log v_{out}/v_{in} \]
Problem 8 [20 points]: Differential Amplifiers

a) Consider the basic differential amplifier circuit shown below. The MOSFETs are long-channel devices.

i) Why should the circuit be symmetric, ideally? [2 pts]

\[ \text{to achieve zero common-mode gain} \]

ii) Can the differential voltage gain, \( v_{\text{out}} / (v_{\text{in1}} - v_{\text{in2}}) \), be adjusted by adjusting the tail current \( I_{\text{SS}} \)? Explain briefly. [3 pts]

\[ \text{YES. The transistor bias currents are each equal to } \frac{I_{\text{SS}}}{2}. \text{ Thus } g_m \propto \sqrt{I_{\text{SS}}} \text{ and hence the voltage gain is } \propto \sqrt{I_{\text{SS}}}. \]

b) Consider the amplifier stage shown below. Assume \( \lambda \neq 0, g_{m/s} > 1 \), and saturation mode operation for each MOSFET.

i) Derive an expression for the differential voltage gain, \( v_{\text{out}} / (v_{\text{in1}} - v_{\text{in2}}) \). [4 pts]

\[ A_v = -g_m \left( \frac{1}{g_{m3}} \right) \frac{R_o}{R_s} \]

ii) Qualitatively, how would the differential voltage gain be affected if the current source \( (I_{\text{SS}}) \) were not ideal, i.e. it had finite resistance? [3 pts]

So long as the circuit is symmetric, the non-ideality of the tail current source will have no impact.

iii) Considering your answer to part (i), what is the best way to adjust the design of this amplifier to increase the voltage gain? (Consider the various options: adjustment in \( I_{\text{SS}}, V_{\text{DD}}, (W/L)_1 \) or \( (W/L)_2 \). Also, consider the trade-off (if any) with the maximum differential input voltage, \( \Delta V_{\text{in, max}} \), which is proportional to \( (V_{\text{GS}} - V_{\text{TH}})_{\text{equil}} \). [4 pts]

From part (i), we see that \( A_v \) can only be adjusted by adjusting \( (W/L)_1 \) or \( (W/L)_3 \).

If \( (W/L)_1 \) is increased, \( \Delta V_{\text{in, max}} \) decreases, which is undesirable.

Thus, the best way to increase \( A_v \) is to decrease \( (W/L)_3 = (W/L)_4 \).

c) What is the benefit of using an active load configuration, as shown to the right? [4 pts]

It allows a single-ended output voltage signal with higher gain and immunity to noise (in \( V_{\text{DD}} \) and \( v_{\text{in1}} \& v_{\text{in2}} \)).
Problem 9 [20 points]: Advanced Topics

a) Illustrate on the plot how the frequency response of an amplifier stage would change with negative feedback, for a loop gain of 10. Estimate the reduction in low-frequency gain. [4 pts]

- Negative feedback lowers the gain by \((1+KA_f)\approx 10\) loopgain.
- Negative feedback enhances the bandwidth by \((1+KA_f)\).

b) Indicate in the table below how CMOS technology parameters should evolve with technology advancement, in order to improve the speed (i.e. reduce the gate delay) of digital CMOS circuits. Assume that transistor channel dimensions \(W\) and \(L\) are scaled proportionately with the gate-oxide thickness. [4 pts]

<table>
<thead>
<tr>
<th>CMOS Technology Parameter</th>
<th>Parameter should</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate-oxide thickness, (T_{ox})</td>
<td>increase</td>
</tr>
<tr>
<td>Carrier mobility, (\mu)</td>
<td>√</td>
</tr>
<tr>
<td>Threshold voltage, (V_{TH})</td>
<td>√</td>
</tr>
<tr>
<td>Power supply voltage, (V_{DD})</td>
<td>√</td>
</tr>
</tbody>
</table>

- Note that this is not good for power density!

c) What is the benefit of using silicon-germanium (SiGe) in the base region of a BJT? Explain briefly. [4 pts]

SiGe has a smaller bandgap energy, hence much larger \(n_t\), than Si.

\[
\beta = \frac{n_{ie}^2 N_e}{n_{ie}^2 N_B} \text{ is therefore enhanced if SiGe is used as the base material.}
\]

This allows large \(\beta\) to be achieved with large \(N_B\), which is beneficial for reducing base-width modulation i.e. achieving large \(ro\) \(\rightarrow\) large \(g_mro\).

d) What is the benefit of using SiGe in the source and drain regions of a p-channel MOSFET? Explain briefly. [4 pts]

Since the lattice constant is larger for SiGe than for Si, SiGe in the source/drain regions induces compressive strain in the channel region, which enhances hole mobility and hence results in larger \(I_{DSS}\) (hence smaller gate delay for digital CMOS) and larger transconductance (hence larger gain for amplifier applications).

e) Why have BJTs (rather than MOSFETs) been preferred, historically, for radio-frequency circuit applications? Why will this change in the future? [4 pts]

The cutoff frequency \((f_T)\) is higher for BJTs than for MOSFETs. As MOSFETs are scaled down in size, their gate capacitance (\(C_g\)) decreases so that \(g_{m/c_g}\) increases with each new generation of CMOS technology. Thus, MOSFETs are becoming suitable for RF applications.