UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 105: Microelectronic Devices and Circuits

Fall 2007

MIDTERM EXAMINATION #2
Time allotted: 80 minutes

NAME: SOLUTIONS
(print) Last First

STUDENT ID#: ________________

INSTRUCTIONS:
1. Use the values of physical constants provided below.
2. SHOW YOUR WORK. (Make your methods clear to the grader!)
3. Clearly mark (underline or box) your answers.
4. Specify the units on answers whenever appropriate.

PHYSICAL CONSTANTS

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electronic charge</td>
<td>$q$</td>
<td>$1.6 \times 10^{-19}$ C</td>
</tr>
<tr>
<td>Boltzmann's constant</td>
<td>$k$</td>
<td>$8.62 \times 10^{-5}$ eV/K</td>
</tr>
<tr>
<td>Thermal voltage at 300K</td>
<td>$V_T = kT/q$</td>
<td>0.026 V</td>
</tr>
</tbody>
</table>

Note that $V_T \ln(10) = 0.060$ V at $T=300$K

PROPERTIES OF SILICON AT 300K

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band gap energy</td>
<td>$E_G$</td>
<td>1.12 eV</td>
</tr>
<tr>
<td>Intrinsic carrier concentration</td>
<td>$n_i$</td>
<td>$10^{10}$ cm$^3$</td>
</tr>
<tr>
<td>Dielectric permittivity</td>
<td>$\varepsilon_{Si}$</td>
<td>$1.0 \times 10^{-12}$ F/cm</td>
</tr>
</tbody>
</table>

SCORE: 1 __________ / 10

2 __________ / 15

3 __________ / 25

4 __________ / 30

Total: __________ / 80
Problem 1 [10 points]: Cascade Stages

a) Consider the common-emitter amplifier stage below. What is the benefit of using a PNP BJT (rather than a resistor) as the load device? [2 pts]

\[ V_{cc} \]
\[ V_b \]
\[ V_{in} \]
\[ Q_1 \]
\[ Q_2 \]
\[ V_{out} \]

The PNP BJT provides a large load resistance \( r_{o2} \) (beneficial for achieving large voltage gain) without requiring a large voltage drop (\( \sim 0.4V \ll I_e r_0 \)) and therefore provides for more headroom than a resistor.

b) Explain qualitatively why the voltage gain of this stage is improved by using a PNP cascode as shown below. Derive a simplified expression for the voltage gain in terms of the BJT small-signal parameters \( g_m, r_e, r_o, \) etc. [5 pts]

You may assume that \( \beta = gm r_e \gg 1 \) and that \( r_e \ll r_o \) for each of the transistors.

\[ V_{cc} \]
\[ V_{b2} \]
\[ V_{b3} \]
\[ V_{in} \]
\[ Q_1 \]
\[ Q_2 \]
\[ Q_3 \]

The load resistance (seen looking into the collector of \( Q_2 \)) is enhanced by using a PNP cascode as the load.

\[ R_{out2} \approx g_{m2} r_{o2} \left( r_{o3} \parallel r_{m2} \right) \gg r_{o2} \]

\[ A_v = -g_{m1} \left( r_{01} \parallel R_{out2} \right) = -g_{m1} \left[ \left( r_{01} \parallel g_{m2} r_{o2} \left( r_{o3} \parallel r_{m2} \right) \right) \right] \]

\[ = -g_{m1} \left( r_{01} \parallel \beta r_{o2} \right) \]

c) Qualitatively, how should the values of the base bias voltages \( V_{b2} \) and \( V_{b3} \) for the PNP transistors be selected? [3 pts]

- \( V_{b3} \) should be selected so that \( V_{be} \) yields the required DC bias current \( (I_e = I_s \exp \left( \frac{V_{be}}{V_T} \right)) \).

- \( V_{b2} \) should be selected as the highest voltage that guarantees that \( Q_2 \) and \( Q_3 \) are each operating in the active region (to provide a large load resistance).
**Problem 2 [15 points]: Current Mirrors**

Consider the circuit shown below:

The BJTs are of identical design, except for their emitter areas:
- The emitter area of $Q_F$ is equal to the emitter area of $Q_{REF}$
- The emitter area of $Q_1$ is 5 times larger than the emitter area of $Q_{REF}$

a) What is the purpose of the transistor $Q_F$? [3 pts]

$Q_F$ supplies the base current for $Q_{REF}$ and $Q_1$, without drawing much current from the current source ($I_{REF}$) so that $I_{C,REF} \approx I_{REF}$.

b) Derive an expression for $I_{copy}$ in terms of $I_{REF}$, neglecting the effect of the transistor base currents. [4 pts]

Noting that the base-emitter voltages are the same for $Q_{REF}$ and $Q_1$:

$$V_X = V_T \ln \left( \frac{I_{C,REF}}{I_{S,REF}} \right) = V_T \ln \left( \frac{I_{copy}}{I_{S,1}} \right)$$

$$\Rightarrow \frac{I_{C,REF}}{I_{S,REF}} = \frac{I_{copy}}{I_{S,1}} \Rightarrow I_{copy} = \frac{I_{S,1}}{I_{S,REF}} \cdot \left( \frac{I_{C,REF}}{I_{S,REF}} \right) = \frac{5A_e}{A_e} \cdot \frac{5I_{REF}}{I_{REF}} = 5I_{REF}$$

$I_S$ is proportional to emitter area, so $\frac{I_{S,1}}{I_{S,REF}} = \frac{5A_e}{A_e} = 5$.

$\therefore I_{copy} = 5I_{REF}$

c) Considering the effect of the transistor base currents, what is the error in $I_{copy}$? [8 pts]

Assume that $\beta$ is the same for all transistors, and that it is large (so that $I_C \approx I_C$ for each transistor).

$$I_{B,REF} = \frac{I_{C,REF}}{\beta} = \frac{I_{copy}/5}{\beta} \quad I_{B,1} = \frac{I_{copy}}{\beta} \quad I_{C,F} \approx I_{C,REF} = I_{B,REF} + I_{B,1}$$

**KCL at collector of $Q_{REF}$**: $I_{REF} = I_{C,REF} + I_{B,REF} = I_{C,REF} + \frac{I_{C,F}}{\beta}$

$$\Rightarrow I_{REF} = \frac{I_{copy}}{5} + \frac{1}{\beta} \left[ \frac{I_{copy}/5}{\beta} + \frac{I_{copy}}{\beta} \right] = \frac{I_{copy}}{5} \left( \frac{1}{\beta} + \frac{1}{5\beta^2} + \frac{1}{\beta^2} \right)$$

$$I_{copy} = \frac{I_{REF}}{\frac{1}{5} + \frac{1}{5\beta^2} + \frac{1}{\beta^2}} = \frac{\frac{I_{REF}}{5}}{1 + \frac{1}{\beta^2} + \frac{5}{\beta^2}} = \frac{5I_{REF}}{1 + \frac{6}{\beta^2}} \approx 5I_{REF} \left( 1 - \frac{6}{\beta^2} \right)$$

$\therefore$ The fractional error in $I_{copy}$ is $\frac{-6}{\beta^2}$.
Problem 3 [25 points]: Frequency Response
Consider the amplifier stage shown below. Assume that $V_A \neq \infty$ for each transistor, and that each transistor is DC-biased to operate in the active mode.

![Amplifier Stage Diagram]

a) Derive an expression for the low-frequency voltage gain. [4 pts] This is a common-emitter stage. The load resistance (seen looking into the collector of $Q_2$) is $r_{o2}$, which is in parallel (between the output node and AC ground) with $r_{o1}$.

\[
A_{vo} = -g_m \left( r_{o1} \parallel r_{o2} \right)
\]

b) Why is it desirable to minimize the capacitive load ($C_1$)? [3 pts]

The load capacitance results in a pole in the transfer function, i.e., causes the voltage gain to decrease when the signal frequency increases above the pole frequency $\omega = \frac{1}{C}$. Small $C_1$ is desirable to increase the pole frequency, for large bandwidth.

c) Draw the BJT junction capacitances ($C_{b1}, C_{b2}, C_{C1}, C_{C2}, C_{C3}, C_{C4}$) on the circuit diagram above. [6 pts] (Note: The substrate of a PNP BJT is n-type, and so it is biased at $V_{CC}$ to ensure that the collector-substrate junction is never forward-biased.)

d) Use Miller’s theorem to derive an approximate expression for the -3dB bandwidth. Assume that the dominant pole is associated with the output node. [8 pts]

$C_{mu}$ contributes an effective capacitance between the output node and ground, of value $(1 - \frac{1}{A_{vo}})C_{mu} = (1 + \frac{g_m(r_{o1} \parallel r_{o2})}{C_{mu}})C_{mu}$.

This is in parallel with the capacitances $C_{b2}, C_{C3}, C_{C4},$ and $C_L$.

The -3dB bandwidth is the frequency of the pole associated with the output node:

\[
\omega_{bw} = \omega_{po} = \frac{1}{\sqrt{(r_{o1} \parallel r_{o2})(C_{b2} + C_{C3} + C_{C4} + C_L)}} \text{ rad/s}
\]

e) Sketch the Bode plot on the axes provided. Label the low-frequency voltage gain and -3dB bandwidth. [4 pts]

![Bode Plot Diagram]
Problem 4 [30 points]: MOS Devices
a) Shown below is the capacitance-vs.-voltage (C-V) characteristic for an MOS capacitor.

![Diagram of MOS capacitor]

i) Is the silicon n-type or p-type? [1 pt]
This is an NMOS device.

ii) Indicate by drawing a dashed line how the C-V curve would change if the Si dopant concentration were to be reduced.
(Assume that the flatband voltage does not change significantly.) [4 pts]

b) Explain why the current in a long-channel MOSFET does not depend on the drain-to-source voltage \( V_{DS} \), when the MOSFET is operating in the saturation region. [5 pts]

In the saturation region of operation, the inversion layer is "pinched off" near the drain. As \( V_{DS} \) is increased, the voltage dropped across the pinch-off region increases, while the voltage dropped across the inversion does not change (staying constant at \( V_{GS} - V_{TH} \)). Thus, the lateral electric field in the inversion layer does not increase, so that the carrier velocity does not increase, hence current does not change.

c) Indicate in the table below (by checking the appropriate box) how the parameters for a short-channel MOSFET would change, if the body dopant concentration were to be increased (e.g. by a factor of 10). Justify your answers. [9 pts]

<table>
<thead>
<tr>
<th>MOSFET Parameter</th>
<th>Parameter will increase</th>
<th>Parameter will decrease</th>
<th>Parameter will not change</th>
<th>Brief Justification (Qualitative reasoning)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Body effect parameter, ( \gamma )</td>
<td>✓</td>
<td></td>
<td></td>
<td>Capacitive coupling between the channel potential and the body voltage is increased, since ( C_{dep} ) increases</td>
</tr>
<tr>
<td>Transconductance, ( g_m )</td>
<td>✓</td>
<td></td>
<td></td>
<td>( g_m ) is only dependent on ( W, \sigma, ) and ( T_{ox} ) for a short-channel MOSFET, none of these are affected by the body dopant concentration</td>
</tr>
<tr>
<td>Output resistance, ( r_o )</td>
<td>✓</td>
<td></td>
<td></td>
<td>The widths of the source/drain junction depletion regions will decrease, so that these junctions support a smaller fraction of the depletion charge underneath the gate, so drain-induced barrier lowering (decreasing ( V_{TH} ) with increasing ( V_{DS} )) is reduced</td>
</tr>
</tbody>
</table>
d) Consider a long-channel MOSFET of channel length \( L \), whose cross-section is shown below. Assume that \( V_S = V_B = 0 \).

![MOSFET Diagram]

i) Identify the MOSFET operating point on the \( I-V \) characteristic to the right. (Circle the appropriate letter.) Briefly justify your answer. [2 pts]

An inversion layer exists across the entire length of the channel, so that the current depends on both \( V_{DS} \) and \( V_{GS} \).

\[ \Rightarrow \text{Triode region of operation} \]

ii) If the threshold voltage \( (V_{TH}) \) is 0.5 V, what is the gate-to-source bias, \( V_{GS} \)? [2 pts]

The saturation voltage is 1 V (from the plot).

\[ \Rightarrow V_{GS} - V_{TH} = 1 \text{ V} \]

\[ V_{GS} = V_{TH} + 1 \text{ V} = 1.5 \text{ V} \]

iii) Estimate the numerical value of the channel length modulation coefficient, \( \lambda \) [4 pts]

From the plot, \( I_D \) increases from 1 mA to 1.2 mA (i.e., by 20%) in the saturation region, when \( V_{DS} \) increases from 1 V to 2 V.

\[ \lambda (V_{DS} - V_{DSat}) = 0.2 \quad \Rightarrow \lambda = 0.2 \text{ V}^{-1} \]

iv) Indicate by drawing a dashed curve on the plot above how the \( I-V \) characteristic would change, if the gate bias were to be decreased such that \( V_{GS} - V_{TH} \) is reduced by a factor of 2. [3 pts]

\[ V_{GS} - V_{TH} \text{ reduced by a factor of 2:} \]

- \( V_{DSat} \) reduced by a factor of 2
- \( I_{DSat} \) reduced by a factor of 4
- \( \lambda \) is unchanged.