Problem 1 of 3: Answer each question briefly and clearly. (40 points)

1.1 Why circuit nodes with very high impedance matter in terms of frequency response? (4 pts)

because they contribute a large RC term.

1.2 When we say that an amplifier stage is “broadband”, what do we mean? (4 pts)

It is only limited by the $r$'s of the device (no Miller effect).

1.3 Place check marks where appropriate (4 pts)

<table>
<thead>
<tr>
<th>Amp Type</th>
<th>Check if Broadband</th>
<th>Check if high $R_s$</th>
<th>Check if high $R_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CD</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CG</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CE</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CC</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CB</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

MOS Device Data*: (you may not have to use all of these...)

- $\mu_{s}C_{ox} = 50 \mu A/V$, $\mu_{s}C_{ox} = 25 \mu A/V$, $V_{TS} = -V_{TH} = 1 V$, $L_{min} = 2 \mu m$, $V_{GS} = 0$
- $V_{DS} = 0.1 V$, $I_{DS} = 1 \mu m$, and it is otherwise proportional to $1/L$
- $C_{mox} = 2.3 F/\mu m^2$, $C_{pox} = 0.1 F/\mu m^2$, $C_{g} = 0.5 F/\mu m^2$, $C_{pox} = 0.5 F/\mu m^2$, $C_{pmox} = 0.5 F/\mu m^2$
- BJT Device Data**: (you may not have to use all of these...)
- $\beta = 100$, $h = 10^{12} A$, $V_{BE, SAT} = 0.1 V$, $V_{A} = 25 V$, $I_{c} = 50 \mu A$, $C_{g} = 15 F/\mu m$, $C_{pox} = 15 F/\mu m$, $V_{BE} = 0.7 V$, $C_{x} = 2.0 V$

* Except as indicated on the particular problem...
1.4 Choose the most appropriate answer (3pts)
The Open-Circuit Time Constant method can only work properly if:

- there is one dominant pole and no zeros
- zero is an Open Circuit connection
- there is no Miller Capacitance
- the Time is Constant

1.5 In this class we talked about the Miller Approximation. Why is it “approximate”? (4pts)

Because we ignored the current drawn by the Miller cap by the output node.

1.6 Match the SPICE control cards (for the types of analysis) to the plots. (3pts)

(a) DC (b) AC (c) TRAN

Figure 1 Figure 2 Figure 3

1.7 For the n-channel MOS transistor shown below, please mark the two ends of the channel (near the source and near the drain) and indicate whether or not each must be inverted so that this device is in saturation. (4pts)

1.8 What is the “law of the junction” and when does it apply? (4pts)

Law of the junction formula:

\[ P(x) = P_o e^{\frac{V_{th}}{V_{th}} \cdot x} \]

\[ N(x) = N_o e^{\frac{V_{th}}{V_{th}} \cdot x} \]

The basic assumption behind it is...

- Low-level injection

1.9 What are the two (small signal) capacitive components of a forward biased junction? (4pts)

Symbol of first capacitance: \( C_{depletion} \)
Verbal Definition:

depletion capacitance

Symbol of second capacitance: \( C_{diff} \)
Verbal Definition:
diffusion capacitance
1.10 For each of these circuits, calculate the "no-signal" DC-bias point at the nodes A and B, assuming that every MOS device is biased so that \( V_{GSS} = 1.5V \) and every BJT is biased so that \( V_{BE} = 0.7V \). After you have done that, circle the circuit that is the "best" in terms of voltage swing at the input \( A^2 \) and low frequency response, and explain where the other two fall short. (6pts)

<table>
<thead>
<tr>
<th>( V_A )</th>
<th>( V_B )</th>
<th>( V_{in, max} )</th>
<th>( V_{in, min} )</th>
<th>( V_A )</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.7</td>
<td>3.2</td>
<td>3.8V</td>
<td>0.8V</td>
<td>4.7</td>
</tr>
<tr>
<td>3.7</td>
<td>3.2</td>
<td>1.0V</td>
<td>0.8V</td>
<td>4.7</td>
</tr>
<tr>
<td>1.7</td>
<td>3.2</td>
<td>0.8V</td>
<td>0.8V</td>
<td>1.7</td>
</tr>
</tbody>
</table>

Note: The input voltage should not be allowed to go over 5V during the operation of these amps. Assume that all the current sources have a minimum voltage drop of 0.5V.

- Problem 2 of 3: Answer each question briefly and clearly. (25 points)

2.1 Design a Common Base "current buffer" amplifier stage so that it meets the following constraints: Total \( R_{in} > 20\,\text{M}\Omega \) if \( R_L = 50\,\text{k}\Omega \), and an absolute current gain \( |\beta| > 1 \) greater than 0.99, when the stage output is shorted. (Use the simplified formulae that assume that \( R_C > \frac{1}{R_{in}} \), \( \frac{1}{R_C} \gg \frac{1}{R_L} \), \( \frac{1}{R_C} \gg \frac{1}{R_\beta} \), and that the intrinsic current gain, \( A_i = 1 \).) (13pts)

\[
\frac{I_{out}}{I_i} = \frac{R_S}{R_S + \frac{R_F}{g_m}}
\]

\[
g_m = \frac{I_i}{V_i}
\]

\[
\frac{R_F}{R_S + \frac{R_F}{g_m}} \geq 0.99
\]

\[
\frac{R_F}{R_S + \frac{R_F}{g_m}} \geq 0.99 \cdot 0.99
\]

\[
g_m \geq 0.99 \leftarrow I_c \geq \frac{g_m}{R_S} \cdot V_A
\]

\[
I_c \geq 49.5 \mu A
\]

\[
R_{out} = \frac{g_m R_F \cdot (R_f + R_S)}{I_c}
\]

\[
= \frac{I_c}{V_k} \cdot \frac{R_A}{R_c} \cdot \frac{1}{H_2}
\]

\[
= \frac{25}{25} \frac{100}{25} \frac{100}{25} \frac{100}{25}
\]

\[
\Rightarrow R_A \leq 25 \, \Omega
\]

Design results:

- \( R_A = \frac{g_m}{I_c} \)
- \( I_c = 49.5 \mu A \)
- \( V_k = 49.5 \mu A \)
- \( \beta = 25 \)
- \( R_F = 125 \Omega \)
- \( R_S = 50.5 \Omega \)
- \( R_{in} = 250 \Omega \)
- \( R_{out} = \frac{g_m}{R_S} \cdot (R_f + R_S) \approx 25 \, \Omega \)

\[
R_A = 50.5 \, \Omega \quad R_{out} = \frac{g_m}{R_S} \cdot (R_f + R_S) = 25 \, \Omega
\]
2.2 Write the 2-port model of this amplifier, add the $C_s$ and $C_j$ parasitic capacitances at the proper locations and calculate $C_\pi$ (assume that $V_{BE}=2V$). Then, assuming that $R_4=0$ (shorted) find the pole of this amplifier and draw the magnitude and phase Bode plot of the current gain $i_{out}/i_t$ (12 pts).

2-port circuit with capacitors

\[ R_{in} = \frac{1}{g_m} \quad R_{out} \sim \frac{g_m R_t}{(R_t + R)} \]

expression value

\[ C_\pi = g_m \cdot C_f + C_{je} = \frac{g_m \cdot 50 \mu F}{100} \cdot 15 \mu F = 17.5 \mu F \]

Transfer function $i_{out}/i_t$ as a function of $\omega$.

\[ \frac{i_{out}}{i_t} = -\frac{V_{BE}}{R_n + j\omega C_{je}} = -\frac{1}{1 + j\omega \frac{C_{je}}{g_m}} \]

Bode Plots

\[ \omega_n = \frac{g_m}{C_{je}} = \frac{17.5 \mu F}{100} \]

Problem 3 of 3: Answer each question briefly and clearly. (35 points)

3. Please do a complete analysis of this transconductance amplifier as follows. Make sure that you use the transistor parameters shown below.

\[ V_T = -0.7 V \quad V_T = 0.7 V \quad V_{BE} = -0.7 V \]

\[ h_{ije} = 25 \mu A/V^2 \quad h_{ije} = 30 \mu A/V^2 \quad h_{ije} = 60 \mu A/V^2 \]

\[ \lambda_e = 0.05 V^{-1} \quad \lambda_e = 0.05 V^{-1} \quad \lambda_e = 0.05 V^{-1} \]

\[ M_2 = M_{2b} = 40 \Omega \quad M_3 = M_{2a} = 40 \Omega \]

\[ M_4 = M_{4b} = 40 \Omega \quad M_5 = M_{4a} = 40 \Omega \]

1. Calculate $(W/L)_1$ of $M_1$ such that the small-signal transresistance $i_{out}/v_t = 1 mS$.

Assume $R_4 = 0\Omega$ for this part. (7pts)

\[ W = \frac{9m^2}{2h_{ije} I_D} \]

expression value

\[ (W/L)_1 = \frac{9m^2}{2h_{ije} I_D} = 1 mS \]

1 Please make sure that you draw the 2-port, and get the small signal model...
3.2 Calculate the value of \( V_{\text{bias}} \) using the \((W/L)\) calculated in part a so that \( I_{\text{OUT}} = 0\text{A} \). (7pts)

\[ I_{\text{out}} \text{ cannot be } 0\text{A, since the output voltage cannot go as low as zero (M} \text{2 would fall out of saturation!)} \].

Still, we should bias M3 so that it draws 100\( \mu \text{A}\) in steady-state.

\[ I_{\text{D}} = \frac{1}{2} \frac{W}{L} \cdot \text{I}_{\text{bias}} (V_{\text{bias}} - V_{\text{IN}})^2 = 100\mu\text{A} \]

\[ V_{\text{bias}} = V_{\text{IN}} + \sqrt{\frac{2 \cdot I_{\text{D}}}{\frac{W}{L} \cdot \text{I}_{\text{bias}}}} \]

\[ V_{\text{bias}} = 0.9 \text{V} \]

3.3 Calculate the output resistance of this amplifier. (7pts)

\[ P_{\text{D}} = P_{\text{up}} || P_{\text{down}} \]

\[ P_{\text{up}} = \frac{V_{\text{out}} - V_{\text{IN}}}{R_{\text{OUT}}} = 15\Omega \]

\[ P_{\text{down}} = \frac{V_{\text{out}} - V_{\text{OUT}}}{R_{\text{OUT}}} = 10.8\Omega \]

\[ R_{\text{OUT}} = P_{\text{up}} + P_{\text{down}} = 25.8\Omega \]

3.4 Find the maximum and the minimum value of the output voltage, and state which transistor limits it in each case, when unloaded \((R_{\text{L}}=\infty)\). (7pts)

\[ V_{\text{OUT}} = V_{\text{D}} - V_{\text{IN}} \]

<table>
<thead>
<tr>
<th>Expression</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{OUT}} ) max</td>
<td>( V_{\text{D}} - V_{\text{IN}} )</td>
</tr>
<tr>
<td>limited by: ( M_3 ), whose gate is at 3.52V</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{OUT}} ) min</td>
<td>( V_{\text{G}<em>2} - V</em>{\text{IN}} )</td>
</tr>
<tr>
<td>limited by: ( M_2 ), whose gate is at 3.52V</td>
<td></td>
</tr>
</tbody>
</table>

3.5 What is the maximum value of the load resistor \( R_{\text{L}} \) at which the overall transconductance is degraded by 20% from the original value of 1mS? (7pts)

\[ G_{\text{M}} = 9 \text{mS,} \quad \frac{R_{\text{OUT}}}{R_{\text{OUT}} + R_{\text{L}}} = 0.8 \]

\[ \frac{R_{\text{OUT}}}{R_{\text{OUT}} + R_{\text{L}}} = 0.8 \Rightarrow \frac{R_{\text{OUT}}}{R_{\text{L}}} = R_{\text{OUT}} = R_{\text{L}} \max \]

\[ R_{\text{L}} \max = R_{\text{OUT}} \left( \frac{1}{0.8} - 1 \right) \]

\[ R_{\text{L}} \max = 156\Omega \]