## Problem \#1a

$\mathrm{T}=$ tape properly threaded, $\mathrm{M}=$ manual mode (automatic $=\sim \mathrm{M}$ ), $\mathrm{E}=$ end-of-tape present, $\mathrm{S}=$ start pressed, $\mathrm{C}=$ 'tape on' from computer, $\mathrm{R}=$ run tape drive.
$\mathrm{R}=\mathrm{T} \sim \mathrm{E}(\mathrm{MS}+\sim \mathrm{MC})$

## Problem \#1b

(i) Maxterm representation: $\mathrm{F}=[\mathrm{Product} / \mathrm{PI}] \mathrm{M}(6,7,9,10,13,14,15)$
(ii) Minimum S-of-P form: $\sim \mathrm{F}=\mathrm{BC}+\mathrm{A} \sim \mathrm{CD}+\mathrm{AC} \sim \mathrm{D}$
(iii) Minimum P-of-S form: $\mathrm{F}=(\sim \mathrm{B}+\sim \mathrm{C})(\sim \mathrm{A}+\mathrm{C}+\sim \mathrm{D})(\sim \mathrm{A}+\sim \mathrm{C}+\mathrm{D})$

## Problem \#2a



## Problem \#2b



## Problem \#3a



## Problem \#3b

Better to realize $\sim x$ and then De Morgan (fewer gates):
$\sim x=\sim A \sim B \sim C+\sim A \sim C \sim D+\sim B \sim C \sim D+\sim A \sim B \sim D$
$\mathrm{x}=(\mathrm{A}+\mathrm{B}+\mathrm{C})(\mathrm{A}+\mathrm{C}+\mathrm{D})(\mathrm{B}+\mathrm{C}+\mathrm{D})(\mathrm{A}+\mathrm{B}+\mathrm{D})$
$y=A B C+A C D+B C D+A B D$


## Problem \#4a

$\mathrm{f} 1=(\mathrm{A} \sim \mathrm{B}+\sim \mathrm{AB})=\mathrm{A}(+) \mathrm{B}$
$\mathrm{f} 2=\mathrm{AB}+\mathrm{f} 1 \mathrm{C}=\mathrm{AB}+\mathrm{C}(\mathrm{A} \sim \mathrm{B}+\sim \mathrm{AB})=\mathrm{AB}+\mathrm{C}(\mathrm{A}(+) \mathrm{B})$
$\mathrm{f} 3=\mathrm{f} 1 \sim \mathrm{C}+\sim \mathrm{f} 1 \mathrm{C}=\mathrm{f} 1(+) \mathrm{C}=\mathrm{A}(+) \mathrm{B}(+) \mathrm{C}$

## Problem \#4b



## Problem \#5a

| Qn | J | $K Q n+1 E n$ |  |  |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
|  | 1 |  | 1 | 0 |
|  | 1 |  | 0 | 1 |



## Problem \#5b

Yes, a hazard does exist in the $\mathrm{Q}->\sim \mathrm{Q}$ transition, as shown in the K-map above. It will not cause a problem if the clock pulse is wider than two gate delays. It can be removed by adding the implicant shown in grey above, corresponding to the logic gate below.


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