Problem 1  (16 points)

List the ROM contents in hexadecimal to implement the FSM shown below. The inputs A and B are synchronized. The states are assigned numerical order, e.g., for state S4, Q2Q1Q0 = 1002. (Follow normal state diagram assumptions: holding in the same state is implicit, etc.).

Fill in ROM contents in hexadecimal. (Binary answers will receive no credit.)

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Fill in ROM contents in hexadecimal. (Binary answers will receive no credit.)
Problem 2  (20 points)

Your lab partner has designed the following Xilinx XC4000 circuit and tells you it works fine in unit delay simulation, but won’t work when downloaded to the Xilinx chip. Given CLKIN=1MHz, $T_{\text{ckmax}}=2.8\text{ns}$, $T_{su}=2.4\text{ns}$.

(a) Complete the timing diagram (considering propagation and interconnect delays) to show why the circuit does not operate as intended.

(b) Circle the problem area(s) in the timing diagram, and briefly explain in a full sentence what the problem is.

(c) Modify the design above so it will work as intended. Do not add any gates or FF.

Problem 3  (50 points)

You are given the 8-bit data path below. The SRAM is $256 \times 8$, but has the same operating characteristics as the static RAM used in lab. 8-bit binary counter CB8RE has synchronous reset.