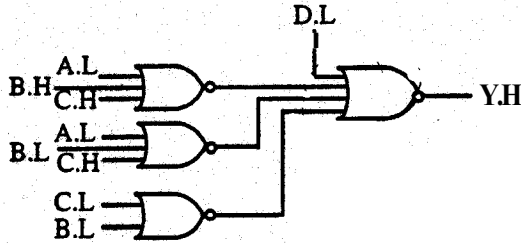
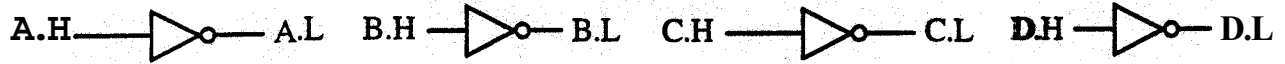
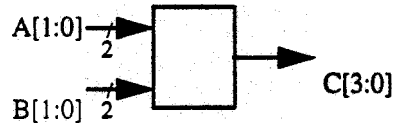


**[8 pts.] a)** You are given the logic diagram below. Complete the truth table for  $Y.H = f(A, B, C, D)$ . Hint: Bubble matching and simplify.



D	C	B	A	$Y = f(A, B, C, D)$	D	C	B	A	$Y = f(A, B, C, D)$
0	0	0	0		1	0	0	0	
0	0	0	1		1	0	0	1	
0	0	1	0		1	0	1	0	
0	0	1	1		1	0	1	1	
0	1	0	0		1	1	0	0	
0	1	0	1		1	1	0	1	
0	1	1	0		1	1	1	0	
0	1	1	1		1	1	1	1	

**[7 pts.] b)** In this problem you will design a combinational circuit that outputs  $C[3:0]$ , which is the product of two 2-bit binary numbers  $A[1:0]$  and  $B[1:0]$ , as shown in the block diagram below.



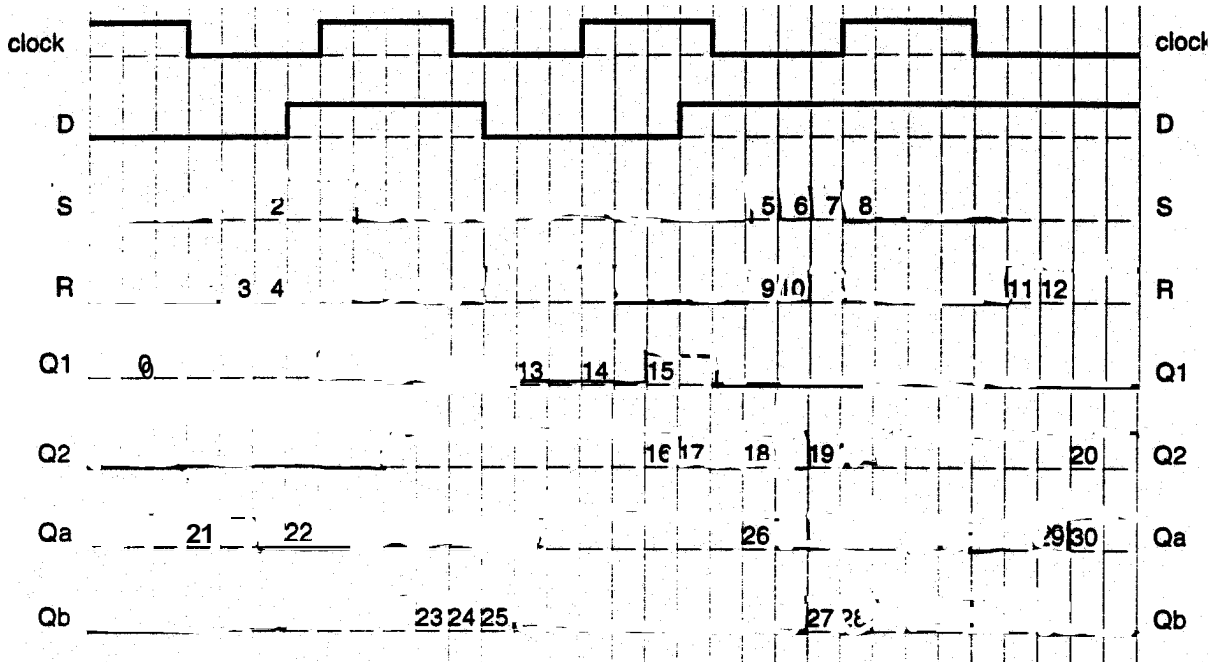
The multiplier is built from an appropriate interconnection of 1-bit multipliers and 1 bit full adders:



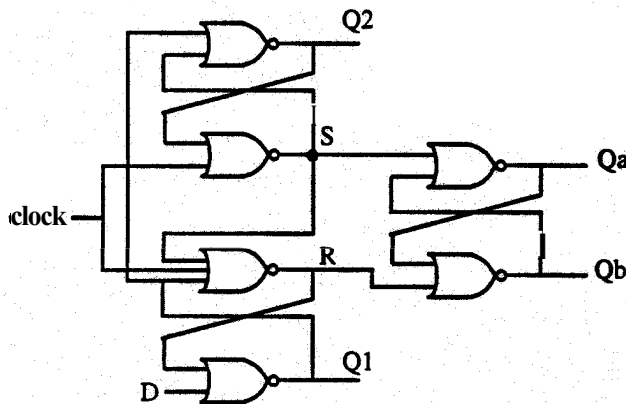
Show how the 1-bit multiplier and full adder modules would be interconnected, using only wires, but no extra gates or inverters.

**Problem 2 (30 points)**

Complete the timing diagram for the figure below, assuming unit delays for all gates and inverters (transport delay only), and no delay in the wires. (The dashed lines in the diagram represent missing sections of the timing diagram.) Complete the table below with the voltage levels at the specified location in the timing diagram, i.e., **L** for low and **H** for high. Example: At location 0, the appropriate voltage level is H. (This problem will be graded +1 for correct, 0 for blank, and -1 for incorrect, with minimum score of 0 points.)

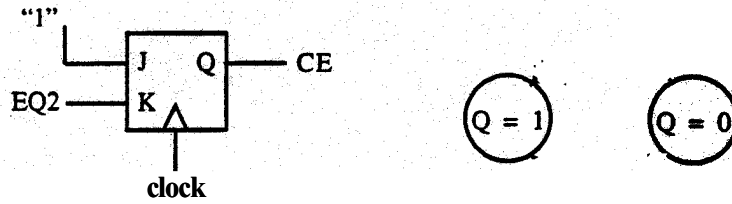


1		6		11		16		21		26	
2		7		12		17	L	22		27	
3		8		13		18		23		28	
4		9		14		19		24		29	
5		10		15		20		25		30	

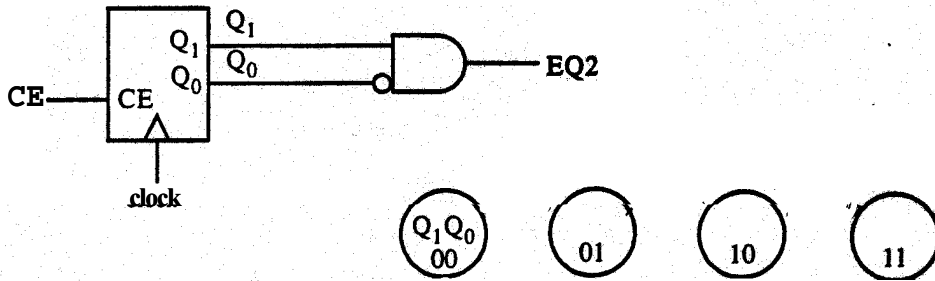


**Problem 3 (15 points) FSM Analysis**

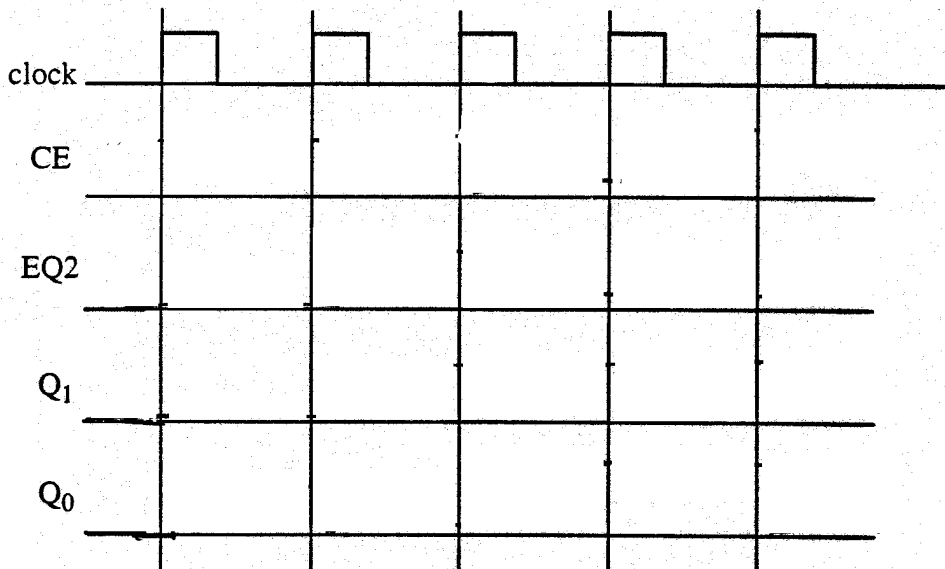
[2 pts.] a) Complete the state diagram for the following FSM, independently of part b):



[3 pts.] b) Complete the state diagram for the following 2-bit binary up counter FSM, independently of part a):



[10 pts.] c) Draw a functional timing diagram for the two FSMs above connected together with common clock, CE(a) tied to CE(b), and EQ2(a) tied to EQ2(b).

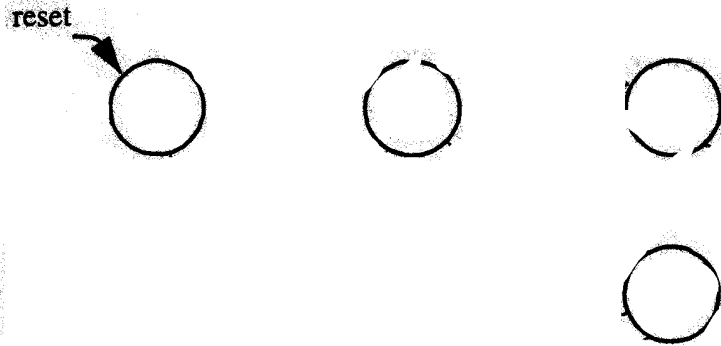


**Problem 4 (?? points)**

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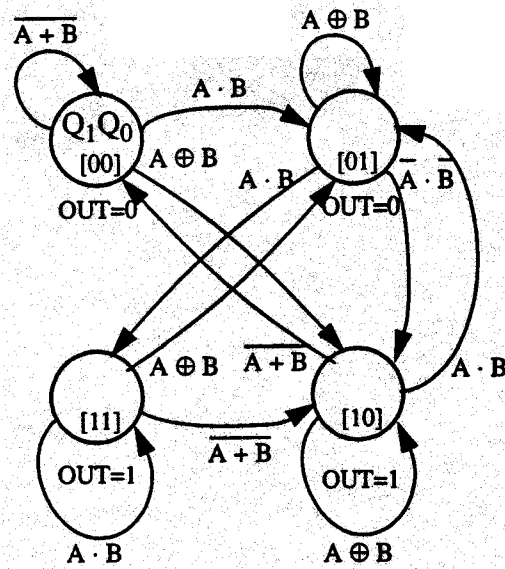
[0 pts.] a) Design a state diagram for a Mealy FSM with synchronized input Z.H and output F.H, which recognizes possibly over-lapping patterns of 101 or 110. For example, if  $Z = 101101$ , then output  $F = 001011$ .

Complete the state diagram for the Mealy sequence recognizer:



**Problem 5 (?? points)**

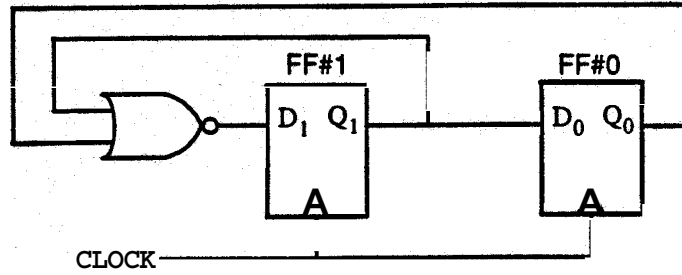
You are given the following state diagram:



Complete the state table for this state diagram.

Present State		Inputs		Next State		Output
Q <sub>1</sub>	Q <sub>0</sub>	A	B	Q <sub>1</sub>	Q <sub>0</sub>	OUT
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

**Problem 6 (20 points)**

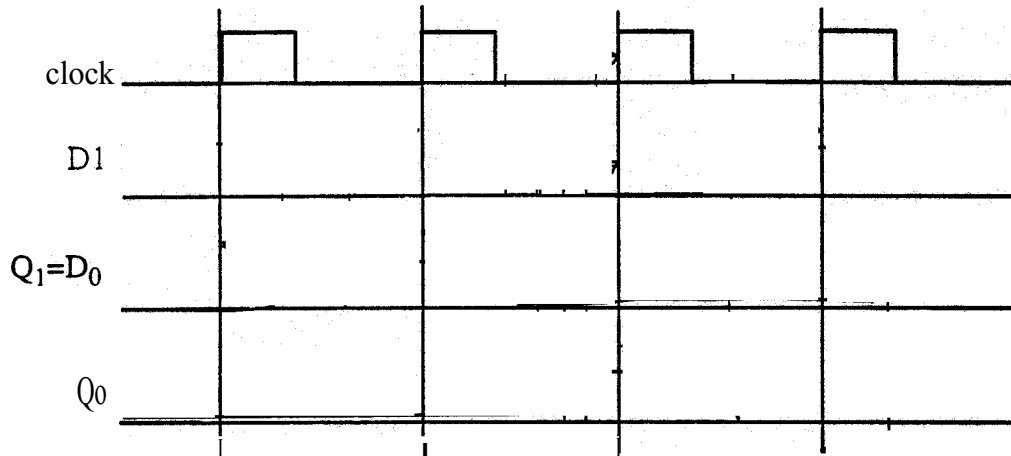


Data:

	FF #1	FF #0
hold time	$t_{h1} = 4 \text{ ns}$	$t_{h0} = 8 \text{ ns}$
setup time	$10 \text{ ns}$	$t_{s0} = 20 \text{ ns}$
propagation delay through FF	$5 < t_{ck1} < 9 \text{ ns}$	$10 < t_{ck0} < 18 \text{ ns}$

propagation delay through NOR:  $7 < t_{NOR} < 12$

[14 pts.] a) Complete a detailed timing diagram (assuming maximum delays) for the FSM above using given timing data. Show all critical delays, labelling in symbolic form, i.e.,  $t_{cko}$  not 18 ns.



[3 pts.] b) What is the minimum clock period (assuming maximum delays) for proper operation of this FSM?

ns

[3 pts.] c) If the clock period = 1000ns, will this FSM operate correctly? Why or why not?