Department of Electrical Engineering and Computer Sciences
College of Engineering
University of California, Berkeley

SR Sanders Spring 2002

EECS40 - Midterm #1

Feb. 26, 2002

Name: _____ **SID#** _____
Last, First

Signature: _____ **TA**:

Guidelines

1. Closed book, except 2 sheets of your own notes.
2. You may use a calculator.
3. Do not unstaple the exam.
4. Show all your work and reasoning on the exam to receive full or partial credit.
5. The exam has 4 problems.

Problem	Points possible	Your score
1	**20**	
2	**20**	
3	**30**	
4	**30**	
total		

1. Consider the Boolean expression:

$$F = (X + \overline{Y})\,(Y + Z)$$

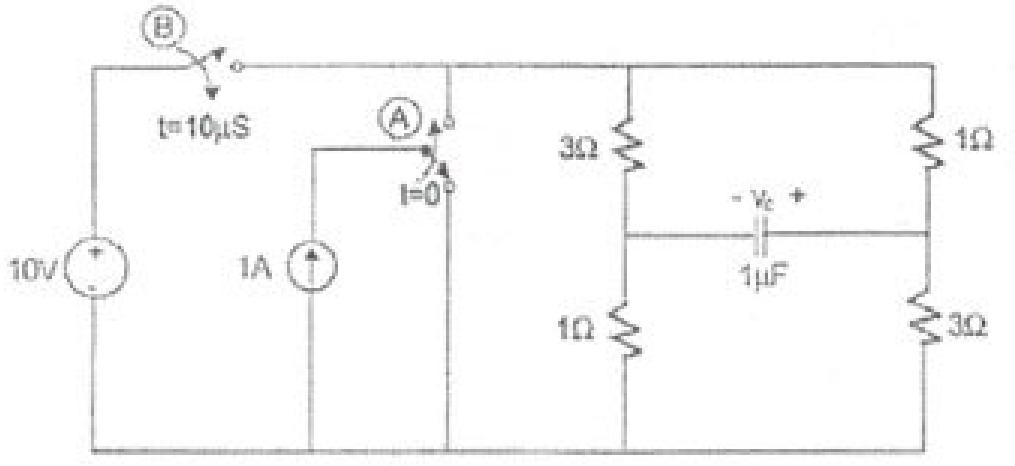
(10) a) Write a truth table for this expression.

X	**Y**	**Z**	**F**
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(10) b) Express F in sum of products form. Do not simplify.

(10) c) Draw a realization for your expression in (b) using NAND logic.

4.



The circuit shown here is at equilibrium with $v_c = 0$ at t = 0. At t = 0, switch A is moved as shown in the diagram. Then at time t = 10 μS, switch B is closed.

(6) a) For time $0 < t < 10$ μS, determine the circuit time constant.

(6) b) Determine an expression for the capacitor voltage for time $0<t<10$ μS.

(6) c) For time t > 10 μS, determine the circuit time constant.

(6) d) Determine an expression for the capacitor voltage $v_c(t)$ for t > 10 μS.

(6) e) Graph v_c (t) for t > 0 on the axes below.