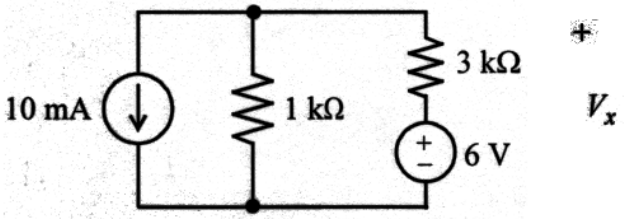
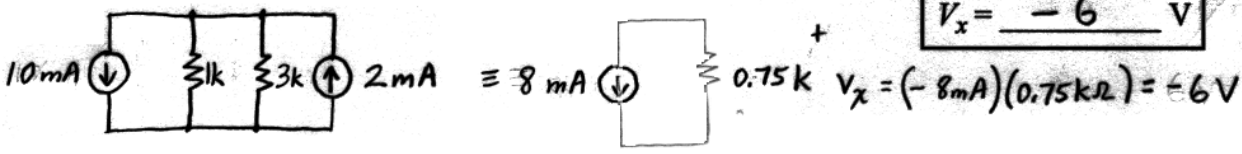
Problem 1: Circuit Analysis [35 points]

a) Find V_x. **[5 pts]**

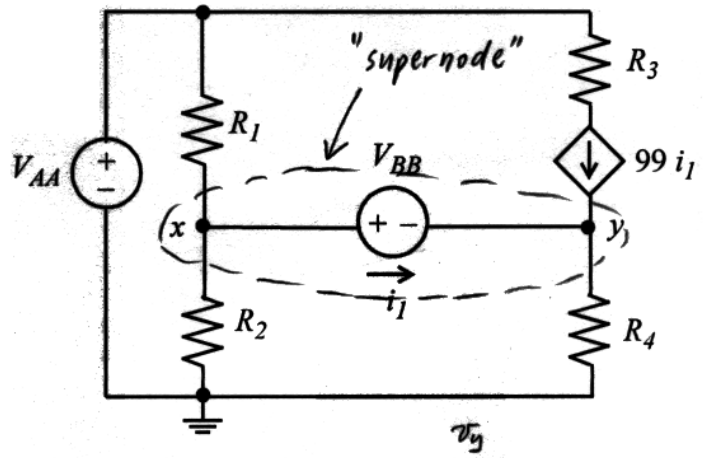


Source transformation:



$V_x =$ **−6** V

b) In the circuit below, the independent source values and resistances are known.
Use the **nodal analysis technique** to write **2 equations sufficient to solve for v_x and v_y.**
To receive credit, you must write your answer in the box below. **[10 pts]**



Apply KCL to node y:

$$99i_1 + i_1 - \frac{v_y}{R_4} = 0$$

$$\Rightarrow i_1 = \frac{v_y}{100R_4}$$

Apply KCL to supernode:

$$\frac{V_{AA} - v_x}{R_1} - \frac{v_x}{R_2} + 99i_1 - \frac{v_y}{R_4} = 0$$

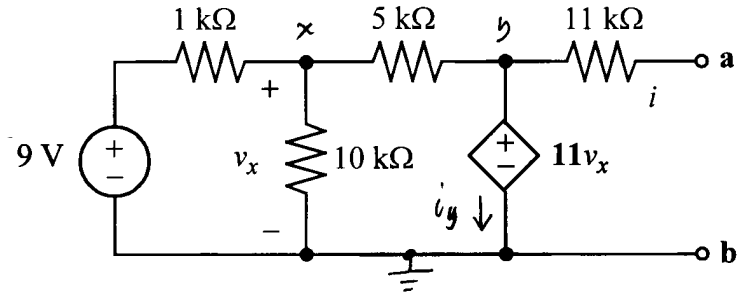
Write the nodal equations here: Need to write equations with only v_x & v_y as unknowns

$$\frac{V_{AA} - v_x}{R_1} - \frac{v_x}{R_2} - \frac{v_y}{100R_4} = 0$$

$$V_{BB} = v_x - v_y$$

Problem 1 (continued)

c) Consider the following circuit:



i) Find the numerical value of v_x. **[5 pts]**

Apply KCL to node x:

$$\frac{9 - v_x}{1k\Omega} - \frac{v_x}{10k\Omega} + \frac{11v_x - v_x}{5k\Omega} = 0$$

$$90 - 10v_x - v_x + 20v_x = 0 \quad \Rightarrow -9v_x = 90 \quad \Rightarrow \quad v_x = -10\ V$$

$v_x =$ **−10** V

ii) Find the power development/absorbed by the dependent source. **[5 pts]**

Current i_y flowing through dependent source is equal to current flowing through 5kΩ resistor.

$$i_y = \frac{v_x - v_y}{5k\Omega} = \frac{v_x - 11v_x}{5k\Omega} = -\frac{10v_x}{5k\Omega} = \frac{100V}{5k\Omega} = 20mA$$

power absorbed $= v_y i_y = (-110V)(20mA) = -2200mW$ → power is developed!

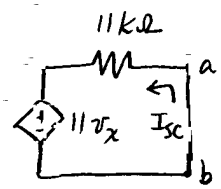
power = 2.2 W

[developed, absorbed]

(circle correct choice)

iii) Draw the Thevenin Equivalent Circuit. **[6 pts]**

Shorting terminals a and b together:

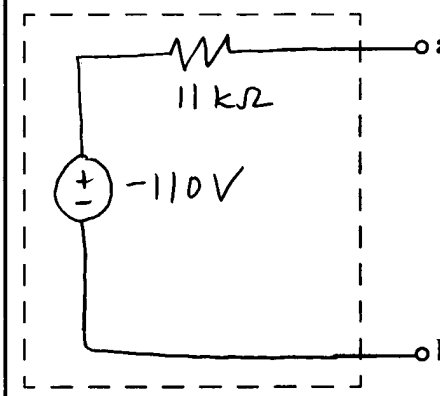


$$I_{sc} = \frac{-11v_x}{11k\Omega} = \frac{110\ V}{11k\Omega} = 10\ mA$$

($11v_x$ ↙)

$$R_{Th} = -\frac{V_{oc}}{I_{sc}} = -\frac{11(-10)}{10\times10^{-3}} = 11k\Omega$$

Thevenin Equivalent Circuit:



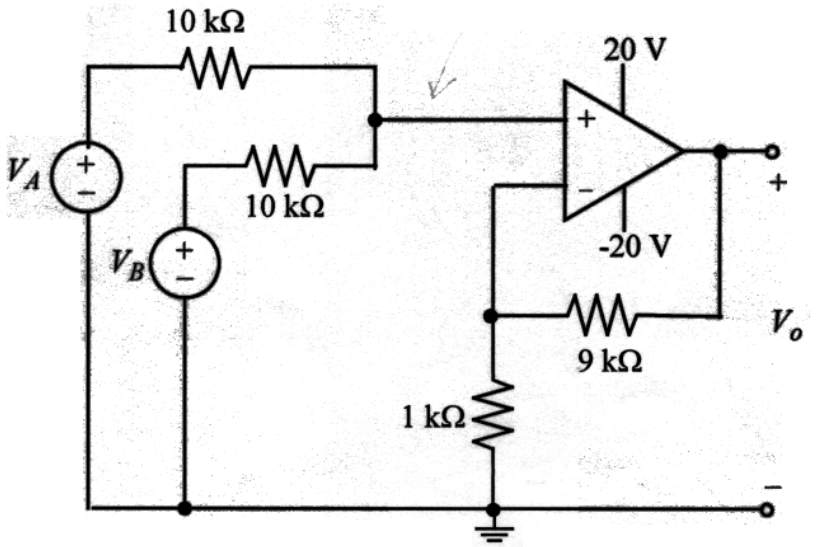
iv) What is the maximum power that can be delivered to a load resistor R_L connected between terminals **a** and **b**? **[4 pts]**

$$\left(\frac{V_{Th}}{2}\right)^2 / R_{Th} = \frac{(55)^2}{11\times10^3} = 275mW$$

Problem 2: Op-Amp Circuits [25 points]

Assume the op-amps in this problem are ideal.

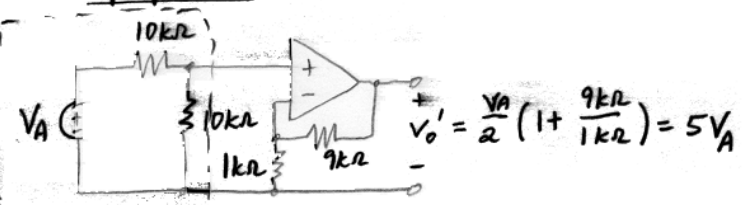
a) Consider the following circuit:

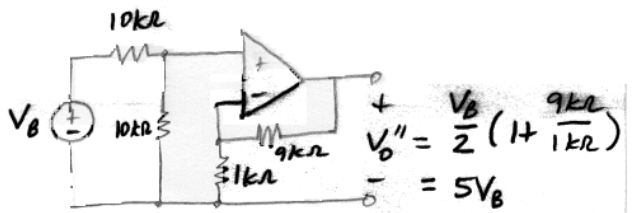


i) Find an expression for V_o. **[10 pts]**

Superposition:

Since no current flows into op-amp input terminal, we can use the voltage-divider formula





$V_o = V_o' + V_o''$

Expression for V_o: $5(V_A + V_B)$

ii) Find V_o for $V_A = V_B = 3$ V. **[2 pts]**

V_o = 20 V

$V_o = 5(V_A + V_B) = 5(3+3) = 30$ V

But this is higher than $V^+ = 20$V

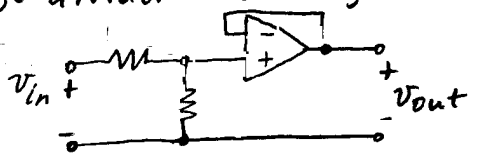
Thus, the op-amp is saturated at 20V

Problem 2 (continued)

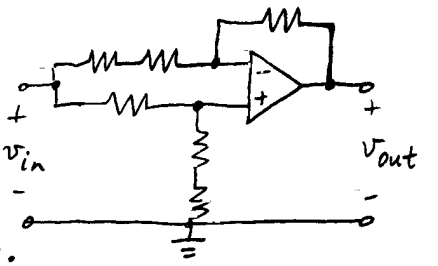
b) i) Design an op-amp circuit which performs the function $v_{out} = 0.5v_{in}$, using only 10 kΩ resistors and op-amps. **[8 pts]**

There are several ways to achieve this:

1) Use a voltage-divider circuit together with a unity-gain buffer:

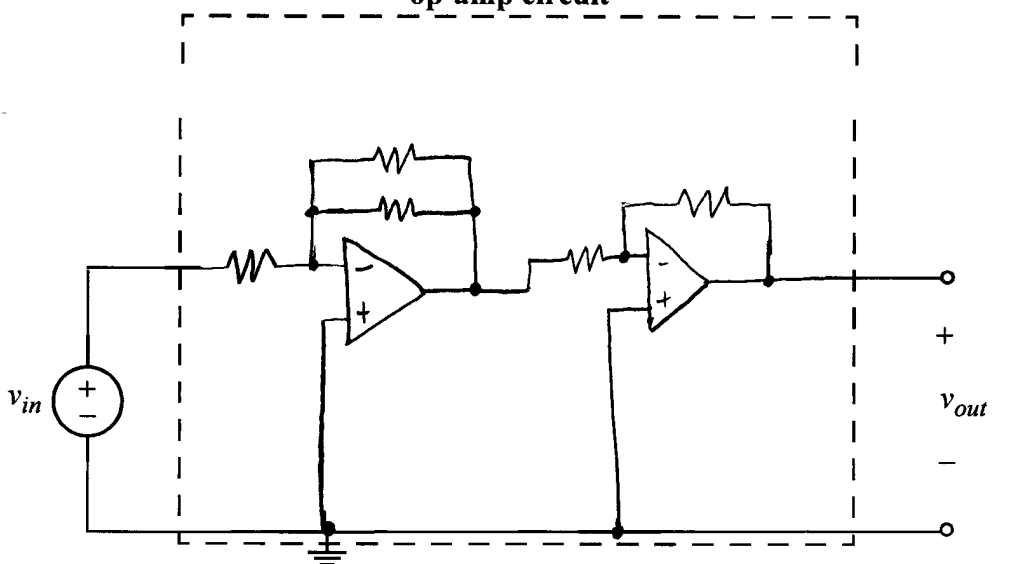


2) Use a differential amplifier circuit:



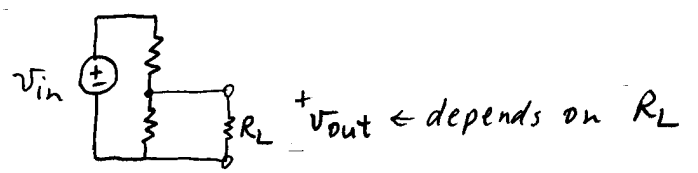
3) Cascade 2 inverting amplifiers, one with gain = −0.5, the other with gain = −1.

op-amp circuit



ii) What is the advantage of using an op-amp circuit to implement this function, rather than using a simple voltage divider (2 resistors connected in series)? **[5 pts]**

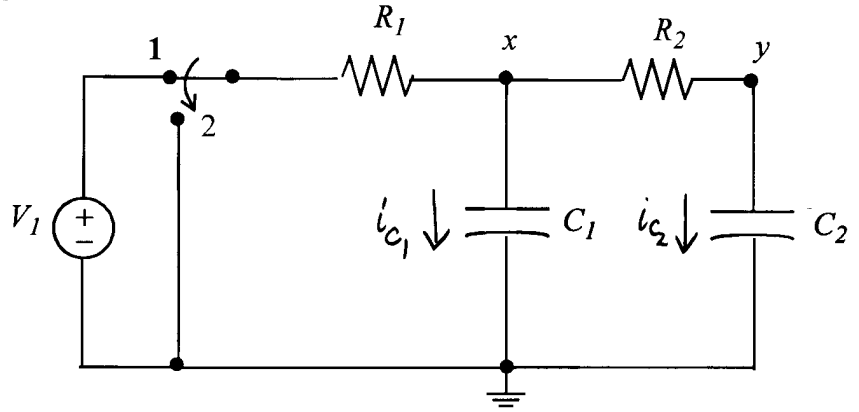
The op-amp circuit doesn't suffer from the loading effect, whereas the simple voltage-divider



← depends on R_L

Problem 3: Transient Response [35 points]

a) In the circuit below, the switch is at position **1** for a long time and is then moved to position **2** at $t = 0$.



For $t<0$, $v_x = v_y = V_1$

$i_{C_1} = C_1 \frac{dv_x}{dt}$

$i_{C_2} = C_2 \frac{dv_y}{dt}$

i) Write 2 independent differential equations relating V_x and V_y, for $t > 0$. To receive credit, you must write your answer in the box below. **[8 pts]**

Applying KCL to node x: $\frac{v_x}{R_1} + C_1 \frac{dv_x}{dt} + \frac{v_x - v_y}{R_2} = 0$ (Equation 1)

Applying KCL to node y: $\frac{v_y - v_x}{R_2} + C_2 \frac{dv_y}{dt} = 0$ (Equation 2)

Write the differential equations here:

$$C_1 \frac{dv_x}{dt} + v_x\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{v_y}{R_2} = 0$$

$$C_2 \frac{dv_y}{dt} + \frac{v_y}{R_2} - \frac{v_x}{R_2} = 0$$

ii) At what rate does V_x change (*i.e.* what is $\frac{dv_x}{dt}$) at $t = 0^+$? **[4 pts]**

At $t=0^+$, $v_x = v_y = V_1$ since voltages across capacitors cannot change instantaneously.

$i_{C_2} = \frac{v_y - v_x}{R_2} = 0 \Rightarrow \frac{dv_x}{dt} = -\frac{v_x}{R_1 C_1} = -\frac{V_1}{R_1 C_1}$

$\frac{dv_x}{dt} = -\frac{V_1}{R_1 C_1}$

iii) At what rate does V_y change at $t = 0^+$? **[3 pts]**

$\frac{dv_y}{dt} = \frac{1}{R_2 C_2}(v_y - v_x) = 0$ (from Equation 1)

$\frac{dv_y}{dt} = 0$

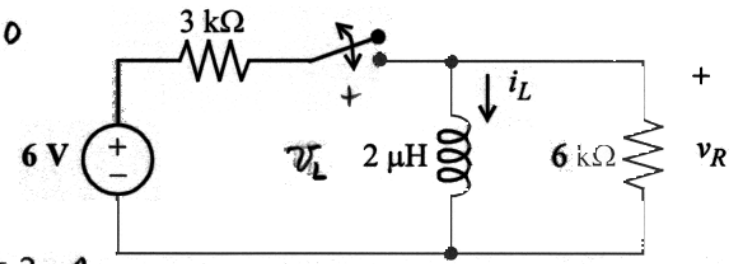
Problem 3 (continued)

b) In the circuit below, the switch has been in the closed position for a long time. The switch is opened at $t = 0$, and then closed again at . $t = 0.5$ ns.

For $t<0$, $\frac{di_L}{dt}=0$ $\Rightarrow v_L = 0$

so 6kΩ resistor is shorted out

$i_L(t<0) = \frac{6V}{3k\Omega} = 2mA$



With switch closed, inductor "sees" 3kΩ resistor in parallel with 6 kΩ resistor:

$R_{eq} = \frac{3\cdot 6}{3+6} = 2\ k\Omega$

i) Write an equation for $i_L(t)$ for $0 < t < 0.5ns$ **[8 pts]**

$\frac{L}{R} = \frac{2\times10^{-6}}{6\times10^{3}}$

$i_L(0^+) = i_L(0^-) = 2mA$

If switch were to stay open indefinitely, the final value of i_L would be 0.

$i_L(t)$ = final value + (initial value − final value) $e^{-t/(L/R)}$

Equation for i_L: $i_L(t) = 2e^{-3\times10^9 t}$ mA $\quad 0<t<0.5ns$

ii) Write an equation for $i_L(t)$ for $t > 0.5ns$. **[8 pts]**

At $t = 0.5ns^-$ $\quad i_L = 2e^{-(3\times10^9)(0.5\times10^9)}$

$= 2e^{-1.5} = 0.45$

$i_L(0.5ns^+) = i_L(0.5ns^+) = 0.45\ mA$

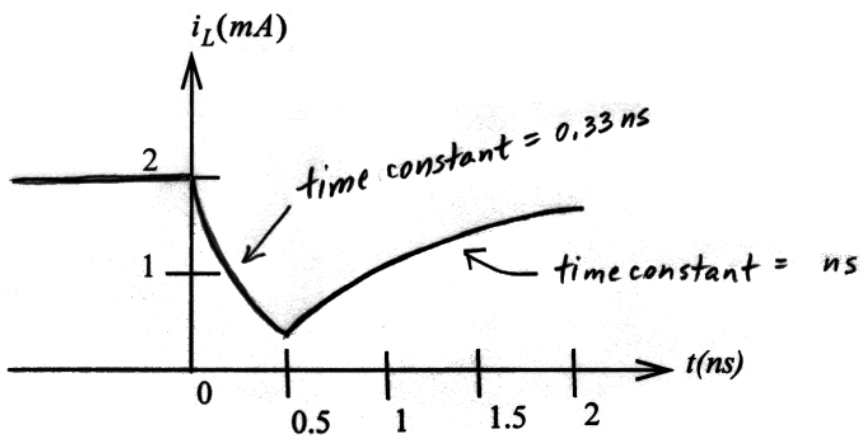
Final value of i_L (switch closed) is 2mA

$i_L(t) = 2 + (0.45 - 2)\, e^{-(t-0.5ns)/(L/R_{eq})}$

$\frac{L}{R_{eq}} = \frac{2\times10^{-6}}{2\times10^{3}} = 10^{-9}s$

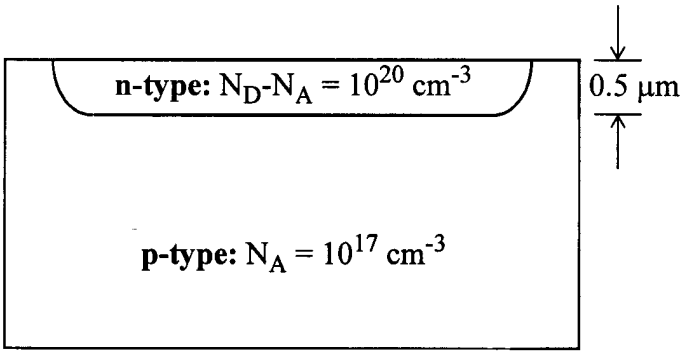
Equation for i_L: $2 - 1.55e^{-10^9(t-0.5ns)}$ mA $\quad t > 0.5ns$

iii) Neatly sketch $i_L(t)$ on the axes provided. **[4 pts]**



Problem 4: p-n Junctions; Diodes [25 points]

a) Consider a p-n junction of area 1 μm^2 formed in a p-type silicon sample maintained at 300K. The p and n regions are uniformly doped, as indicated in the figure below.



Schematic cross-sectional view of p-n junction

i) What is the sheet resistance of the n-type region? **[9 pts]**

n-type region : $n = N_D - N_A = 10^{20} cm^{-3} >> p$

$\frac{1}{q\mu_n n + q\mu_p p} \simeq \frac{1}{q\mu_n n}$

From plot of mobility vs. dopant concentration on Page 2, $\mu_n \simeq 80\ cm^2/Vs$ for $N_A + N_D = 10^{20} cm^{-3}$

$\frac{\rho}{t} = \frac{1}{q\mu_n n t} = \left[(1.602\times10^{-19})(80)(10^{20})(0.5\times10^{-4})\right]^{-1} = 15.6\ \Omega/\square$

$R_s =$ 15.6 Ω/square

ii) What is the junction capacitance? (Consider the worst case: 0V bias voltage.) **[10 pts]**

built-in potential $\phi_{bi} = \frac{kT}{q} \ln \frac{(10^{20})(10^{17})}{(1.45\times10^{10})^2} = 0.99V$

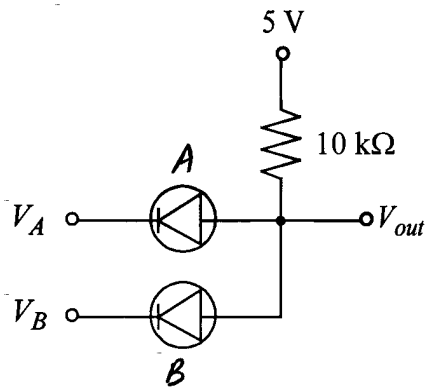
$= \sqrt{\frac{2\varepsilon_{Si}(\phi_{bi} - V)}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} = \sqrt{\frac{2(11.7\times8.854\times10^{-14})(0.99)}{1.602\times10^{-19}}\left(\frac{1}{10^{17}} + \frac{1}{10^{20}}\right)} = 0.113\ \mu m$

$C_j = A\frac{\varepsilon_{Si}}{x_d} = (10^{-4})^2 \frac{(11.7)(8.854\times10^{-14})}{1.13\times10^{-5}} = 9.17\times10^{-16}\ F$

$C_j =$ 0.92 fF

Problem 4 (continued)

b) Consider the following diode (ideal rectifier) circuit:



i) Fill in the table with the values of V_{out} for various combinations of V_A and V_B. **[4 pts]**

$V_A = V_B = 0V$: Both rectifiers are ON, shorting Vout to V_A & V_B

$V_A = 0$, $V_B = 5V$: Only rectifier A is ON, shorting Vout to V_A.

$V_A = 5V$, $V_B = 0V$: Only rectifier B is ON, shorting Vout to V_B.

$V_A = V_B = 5V$: Both rectifiers are on, shorting Vout to V_A & V_B

V_A (Volts)	V_B (Volts)	V_{out} (Volts)
0	0	0
0	5	0
5	0	0
5	5	5

ii) What logic function does this circuit perform? **[2 pts]**
(Assume that 5 V corresponds to logic level 1, and 0 V corresponds to logic level 0.)

Truth table:

V_A	V_B	V_{out}
0	0	0
0	1	0
1	0	0
1	1	1

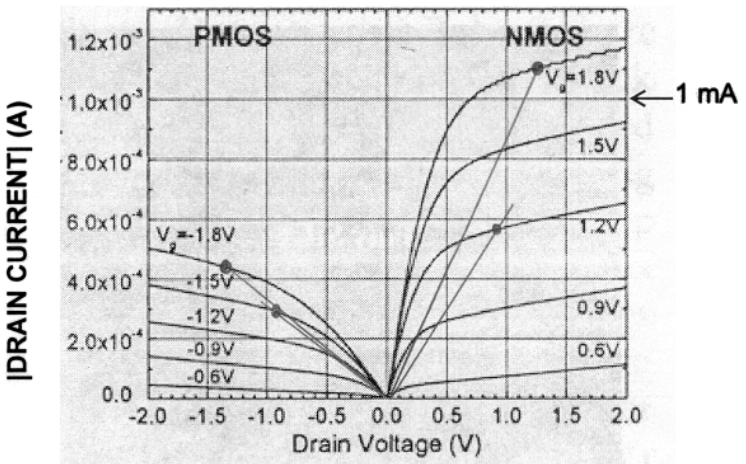
This is an AND gate.

Problem 5: MOSFETs -- Short Answer (1-2 sentences) **Questions [20 points]**

a) Why does drain current $|I_{DS}|$ saturate as $|V_{DS}|$ increases in a short-channel MOSFET? **[5 pts]**

As $|V_{DS}|$ increases, the lateral electric field increases to a high enough level that velocity saturation occurs, in which case the carrier velocity (hence $|I_{DS}|$) doesn't increase with further increases in electric field ($\propto |V_{DS}|$).

b) Given the following CMOS current-vs.-voltage characteristics:



i) Are these short-channel MOSFETs? Justify your answer. **[5 pts]**

Yes. The saturation current increases linearly with fixed increments in $|V_{GS}|$, characteristic of short-channel MOSFETs.

ii) Estimate the equivalent resistances R_n and R_p (relevant for digital CMOS circuits) of the n-channel and p-channel transistors, respectively, for $V_{DD} = 1.8$ V. **[6 pts]**

Find drain currents at $|V_{DS}| = \frac{1}{2}(V_{DD} + \frac{V_{DD}}{2}) = \frac{3}{4}V_{DD}$, for $|V_{GS}| = V_{DD}$.

$= 1.35\,V$

NMOS $I \cong 1.1 \times 10^{-3}\,A$

$R_n = \frac{1.35\,V}{0.0011\,A} = 1227\,\Omega$

PMOS: $I \cong 4.5 \times 10^{-4}\,A$

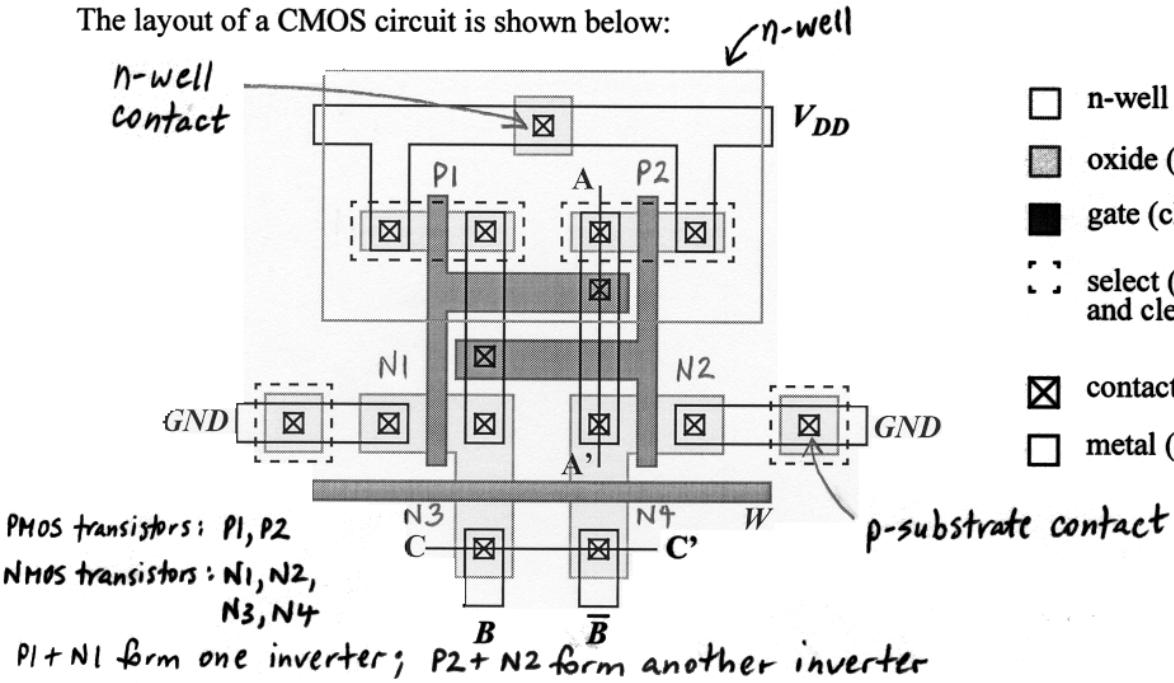
$R_p = \frac{1.35\,V}{4.5 \times 10^{-4}\,A} = 3000\,\Omega$

iii) How will the equivalent resistance change as V_{DD} is reduced (*e.g.* to save power)? What impact would a reduction in V_{DD} have on logic-gate delay? **[4 pts]**

Consider a lower V_{DD}, e.g. 1.2V. Comparing the slopes which represent $\frac{1}{R_{eq}}$ (see I-V plot above), we see that R_{eq} increases as V_{DD} is reduced. Larger R_{eq} $\Rightarrow$ larger RC $\Rightarrow$ increased delay

Problem 6: CMOS Circuit [30 points]

The layout of a CMOS circuit is shown below:



PMOS transistors: P1, P2

NMOS transistors: N1, N2, N3, N4

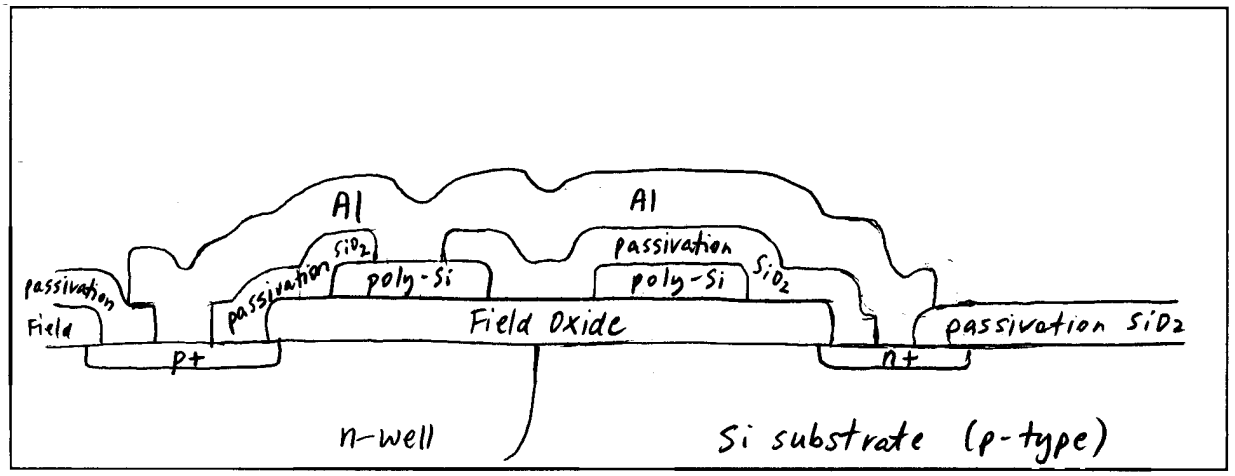
P1 + N1 form one inverter; P2 + N2 form another inverter

The following fabrication process (starting with a p-type Si wafer) is used:

1. Thermally grow 700 nm of SiO_2.
2. Pattern the SiO_2 using the well mask.
3. Implant phosphorus and perform a high-temperature, long anneal to "drive in" the well to a depth of 2 μm.
4. Remove the SiO_2 (using a highly selective wet etch process, which does not etch Si).
5. Grow 500 nm of SiO_2 ("field oxide").
6. Pattern the SiO_2 using the oxide ("active-area") mask.
7. Thermally grow 10 nm of SiO_2 ("gate oxide") in the bare regions of the Si.
8. Deposit 500 nm of heavily doped poly-Si (by CVD).
9. Pattern the poly-Si using the gate mask.
10. Use dark-field select mask to pattern photoresist; implant boron; strip the photoresist. This will form the p+ source and drain junctions for the p-channel MOSFET.
11. Use clear-field select mask to pattern photoresist; implant arsenic; strip the photoresist. This will form the n+ source and drain junctions for the n-channel MOSFET.
12. Anneal the wafer in order to activate the dopants. The final source/drain junction depth is 250 nm.
13. Deposit 500 nm of SiO_2 ("passivation oxide").
14. Pattern the deposited SiO_2 film using the contact mask.
15. Deposit 750 nm of aluminum.
16. Pattern the Al using the metal mask.

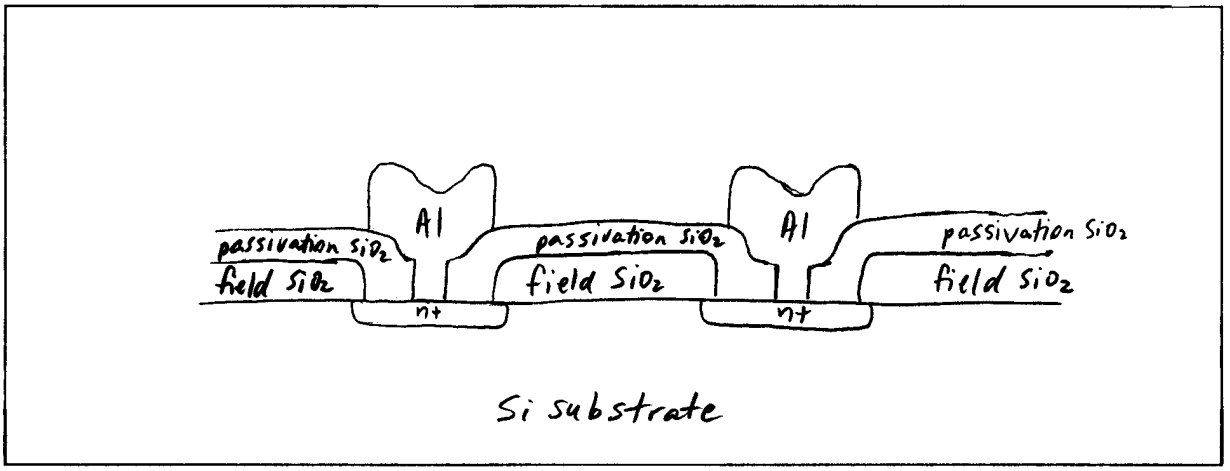
Problem 6 (continued)

a) Draw cross-section A-A' in the space provided. Identify all layers clearly. **[15 pts]**



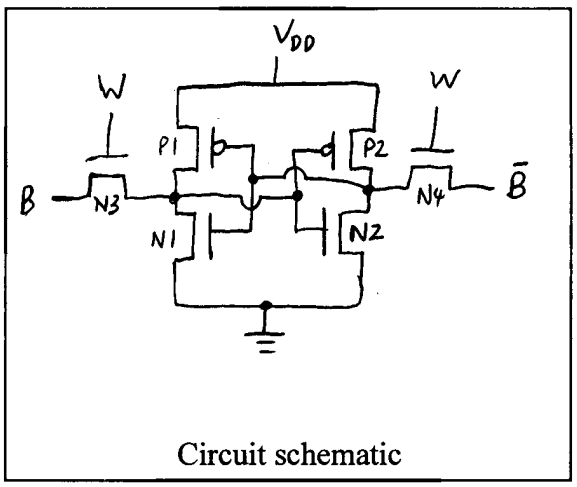
Cross-section A-A'

b) Draw cross-section C-C' in the space provided. Identify all layers clearly. **[10 pts]**



Cross-section C-C'

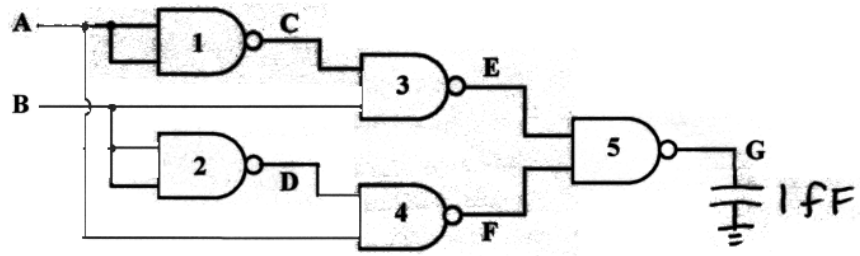
c) Draw the circuit schematic, labelling V_{DD}, GND, W, B and $\overline{B}$. **[5 pts]**



Circuit schematic

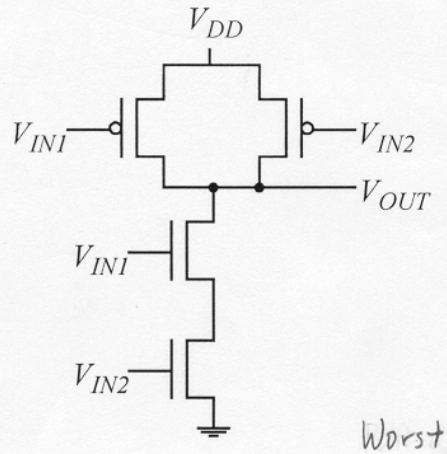
Problem 7: Logic Circuit; Gate Delay Analysis [30 points]

Consider the following logic circuit:



The NAND gate circuit schematic is given below:

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.854\times10^{-14})}{2.5\times10^{-7}} = 1.38\,\mu F/cm^2$



Gate-oxide thickness = 2.5 nm

PMOS:
W/L = 0.3 μm/0.2 μm
R_p = 20 kΩ

NMOS:
W/L = 0.2 μm/0.2 μm
R_n = 10 kΩ

Worst case pull-up (only one PMOSFET ON) resistance = pull-down resistance = 20 kΩ

a) Fill out the truth table, and write a **simple** logical expression for the function G. **[5 pts]**

NAND Truth Table:

0 0	1
0 1	1
1 0	1
	0

A	B	C ($\bar{A}$)	D ($\bar{B}$)	E ($\overline{BC}$)	F ($\overline{AD}$)	G ($\overline{EF}$)
0	0	1	1	1	1	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	0	1	1	0

G = $\bar{A}B + \bar{B}A$ (exclusive OR)

Problem 7 (continued)

b) Compute the delay of the logic circuit (time between an input voltage step change and time at which the voltage at G reaches $0.5V_{DD}$), assuming that the drain-junction and interconnect capacitances are negligible. **[9 pts]**

$C_p = (W_p \times L_p) C_{ox} = (0.3\times10^{-4})(0.2\times10^{-4})(1.38\times10^{-6})$
$= 0.828\,fF$

delay = 51.9 ps

$C_n = (W_n \times L_n) C_{ox} = (0.2\times10^{-4})(0.2\times10^{-4})(1.38\times10^{-6}) = 0.552\,fF$

There are 3 stages in the logic circuit. For the first 2 stages, the load capacitance is $C_n + C_p = 1.38\,fF$. For the 3rd stage, the load capacitance is 1 fF. For all 3 stages, the pull-up/pull-down resistance is 20 kΩ.

$$\text{Delay} = \left[(RC)_{1st\ stage} + (RC)_{2nd\ stage} + (RC)_{3rd\ stage}\right] \times 0.69$$
$$= \left[(20\times10^3)(1.38\times10^{-15}) + (20\times10^3)(1.38\times10^{-15}) + (20\times10^3)(1\times10^{-15})\right] \times 0.69$$
$$= 51.9\ ps$$

c) Compute the delay of the logic circuit again, this time assuming that the interconnects between gates 3 and 5 and between gates 4 and 5 have significant resistance R_{int} = 1 kΩ and capacitance (to ground) C_{int} = 1 fF. (Use the "one-lump" interconnect model.) **[10 pts]**

delay = 67.3 ps

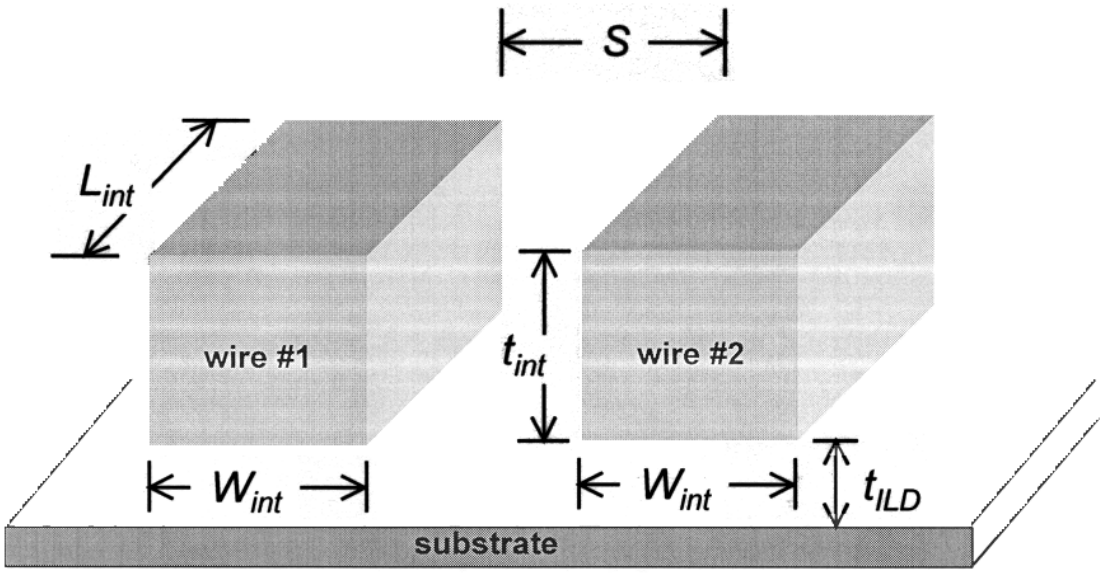
For the 2nd stage, the load capacitance is now $C_{int} + C_n + C_p = 2.38\,fF$, and the pull-up/pull-down resistance is now 20 kΩ + kΩ = 21 kΩ.

$$\text{Delay} = \left[(20\times10^3)(1.38\times10^{-15}) + (21\times10^3)(2.38\times10^{-15}) + (20\times10^3)(1\times10^{-15})\right] \times 0.69$$
$$= 67.3\ ps$$

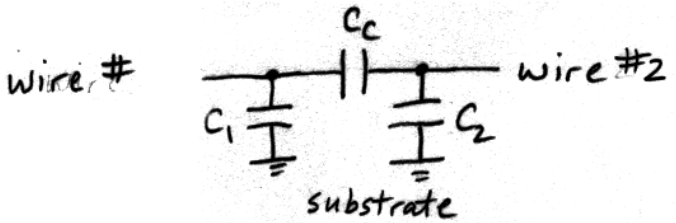
Problem 7 (continued)

d) Consider two interconnect wires which lie close to each other, as illustrated below. When the voltage on one wire changes, the voltage on the other wire will be affected due to capacitive coupling between the two wires; this phenomenon is referred to as "cross-talk".

Indicate in the table below how cross-talk would be affected by various changes. **[6 pts]**



Change:	Cross-talk will: increase	decrease	not change	Brief Explanation/Justification
increase S		✓		coupling capacitance between wires decreases
increase t_{int}	✓			coupling capacitance between wires increases
increase W_{int}		✓		capacitance between wire & ground increases; $\frac{C_c}{C_c+C_2}$ decreases



crosstalk on wire #2 $\propto \frac{C_c}{C_c+C_2}$