UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

Professor Oldham

Fall 1999

EECS 40 — FINAL EXAM

13 December 1999

Name: ______________________________
Last, First

Student ID: _________

TA: ❑ Kusuma
❑ Chang

Guidelines:

(a) One page of notes allowed (both sides).

(b) You may use a calculator.

(c) Do not unstaple the exam.

(d) Show ***all your work and reasoning on the exam*** in order to receive full or partial credit.

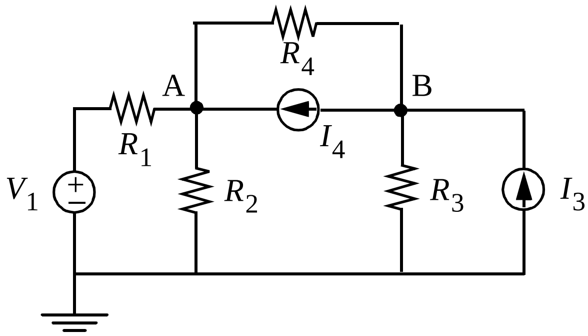
(e) This exam contains 16 pages plus the cover page and 2 sheets of scratch paper included at the end of the exam. You can remove these from the rest of the exam if you wish.

Problem	**Points Possible**	**Your Score**
1	20	
2	25	
3	30	
4	25	
5	25	
6	20	
7	25	
8	30	
Total	**200**	

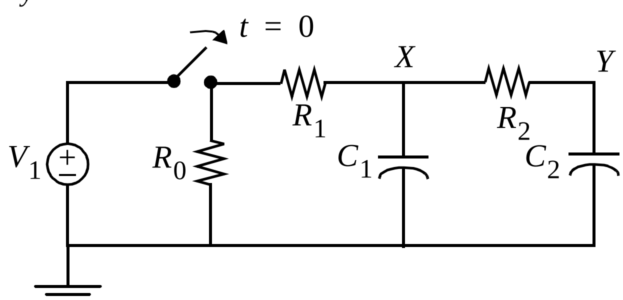
$K = 10^3$
$m = 10^{-3}$
$\mu = 10^{-6}$
$n = 10^{-9}$
$p = 10^{-12}$
$f = 10^{-15}$

Problem 1 Nodal Analysis (20 points)

(a) Write 2 nodal equations sufficient to find voltages A and B.



(b) The switch closes at $t = 0$ (after a very long time open). Write 2 nodal differential equations describing V_x and V_y.



(c) What are the values of V_x, V_y at $t = 0^+$ and $t \to \infty$?

Problem 1 Answers

(a)

(b)

(c)

$V_x(t = 0^+)$ = ______________

$V_y(t = 0^+)$ = ______________

$V_x(t \to \infty)$ = ______________

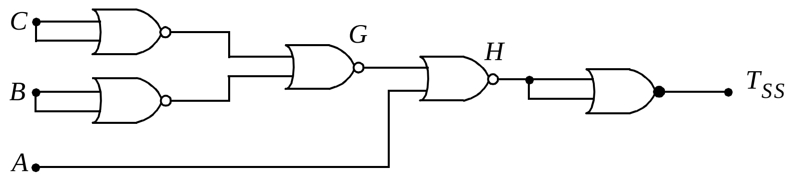
$V_y(t \to \infty)$ = ______________

Problem 2 Nerd Contest (25 points)

In a post-Big Game Nerd Competition, teams from Stanford and UCB were asked to draw logic diagrams to implement the following function:

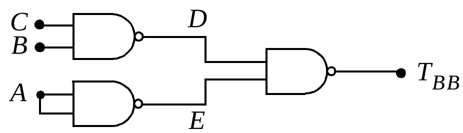
$$T = A + BC$$

The Stanford team came up with the following design based on NOR gates



Design SS

The Berkeley team came up with the following design based on NAND gates:



Design BB

(a) Fill out the truth tables opposite to evaluate T_{SS} and T_{BB}.

(b) Do both circuits function as desired?

(c) Define the unit gate delay of the NOR gates as τ_{NOR} and unit gate delay of the NAND as τ_{NAND}. Assume the outputs, T, are loaded by similar gates. What is the delay of the Stanford circuit and what is the delay of the Berkeley circuit (in terms of τ_{NOR}, τ_{NAND})?

Problem 2 Worksheet and Answers

(a)

FILL OUT
WITH ZEROS
AND ONES

A	**B**	**C**	**G**	**H**	T_{SS}	**D**	**E**	T_{BB}
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

(b)

Function correct?
(yes or no?)

T_{SS} ☐

T_{BB} ☐

(c) Delay

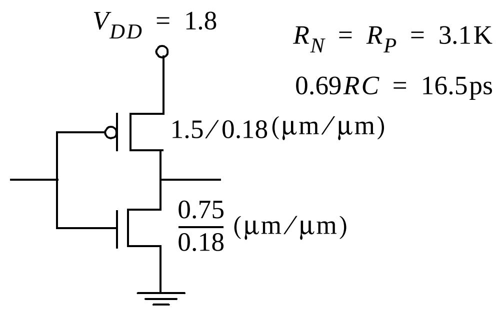
SS Circuit ____________________________

BB Circuit ____________________________

Problem 3 Nerd Contest – Details (30 points) (Independent of Problem 2)

(a) The schematic of a CMOS inverter analyzed in Lecture 25 is shown in the figure below. Note the unit gate delay is 16.5 ps when the inverter drives an identical inverter.

Using the same CMOS technology, you are to design (that means draw the schematic of) a 2-input NAND gate [NOT a layout please!]. Please size the devices for equal worst-case rise and fall times, and use 1.5/0.18 as the p-channel device size.



(b) Find the input capacitance and the output resistance of such a NAND gate (worst case). Compute the gate delay assuming the NAND gate drives an input to identical NAND gates. Ignore drain-bulk and interconnect capacitance.

(c) Now draw the schematic of the NOR gate and indicate device sizes needed to get equal (worst-case) rise and fall times. Again use 1.5/0.18 as the p-channel device size.

(d) Find the input capacitance and the output resistance of such a NOR gate. Compute the unit gate delay assuming the NOR gate drives an input to identical NOR gates. Ignore drain-bulk and interconnect capacitance.

<u>Problem 3 Worksheet and Answers</u>

(a)

schematic of NAND gate

PMOS $\frac{W}{L} = \frac{1.5}{0.18}$

NMOS $\frac{W}{L} = $ ______

(b) C_{GP} = ________________fF C_{GN} = ________________fF

R = ________________K   Unit Gate Delay = ________________pS

(c)

schematic of NOR gate

PMOS $\frac{W}{L} = \frac{1.5}{0.18}$

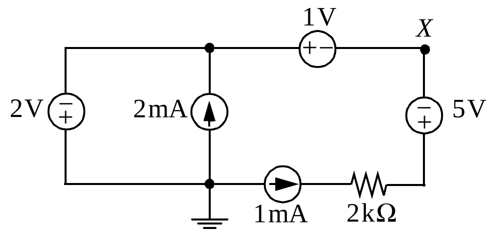
NMOS $\frac{W}{L} = $ ______

(d) C_{GP} = ________________fF C_{GN} = ________________fF

R = ________________K   Unit Gate Delay = ________________pS

Problem 4 Simple Circuits (25 points)

(a)

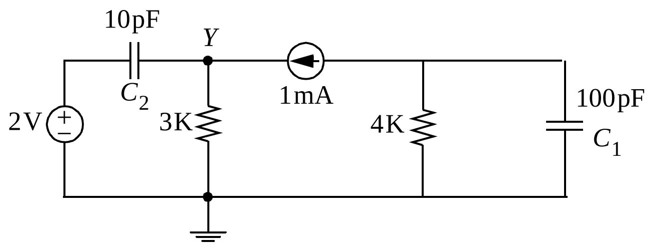


V_X = ______

Power delivered by 1mA source = ______

Power delivered by 2mA source = ______

(b)

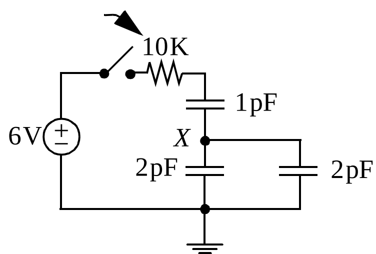


V_Y = ______

Power delivered by 1mA source = ______

Energy stored in C_2 = ____________

(c)

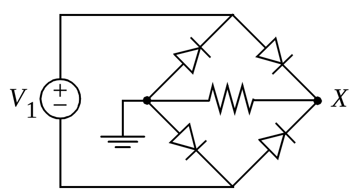


Capacitors are initially uncharged. Find V_X long after the switch is closed. Find peak power P_{MAX} delivered by the voltage source.

V_X = ________________

P_{MAX} = ________________

(d)

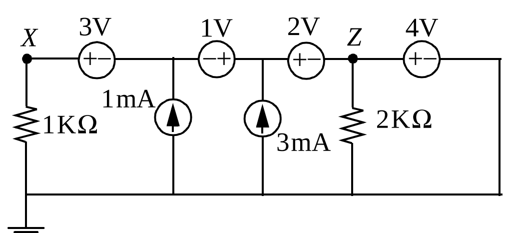


Assume the 4 diodes are perfect rectifiers. (a) What is V_X when $V_1 = 5V$? (b) What is V_X when $V_1 = -5V$?

a) V_X = ________________

b) V_X = ________________

(e)

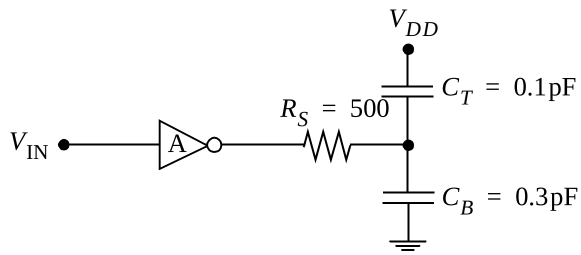


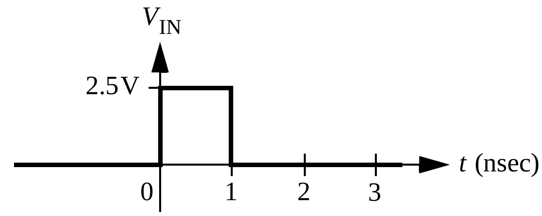
V_X = ________________

V_Z = ________________

Problem 4 Worksheet

Problem 5 Inverter Transient (25 points)





Inverter A is a CMOS inverter with effective output resistance of 1.5K. $V_{DD} = 2.5\text{V}$ and $V_{Tl} = 0.7$, $V_{Th} = 1.8\text{V}$.

The input capacitance of inverter A is 5 fF, V_{IN} was zero for $t < 0$, then a pulse generator (with very low output resistance) produces the input waveform shown above.

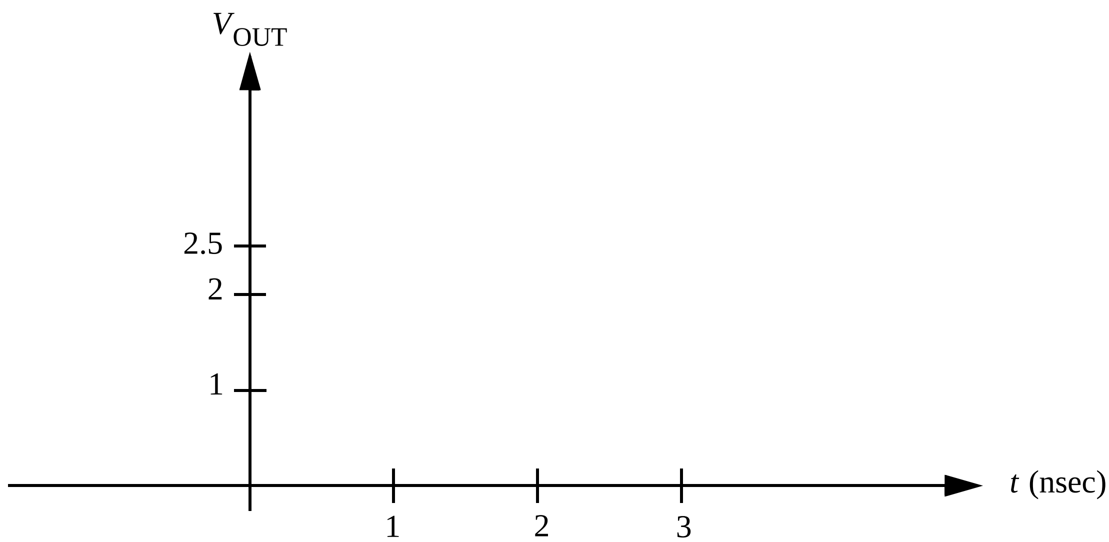
(a) Sketch the general form of $V_{OUT}(t)$.

(b) Calculate V_{OUT} at $t = 0+$, $t = 1$ nsec, and $t = 2$ nsec.

(c) Re-sketch $V_{OUT}(+)$ very carefully and neatly.

Problem 5 Answer Sheet

(a)



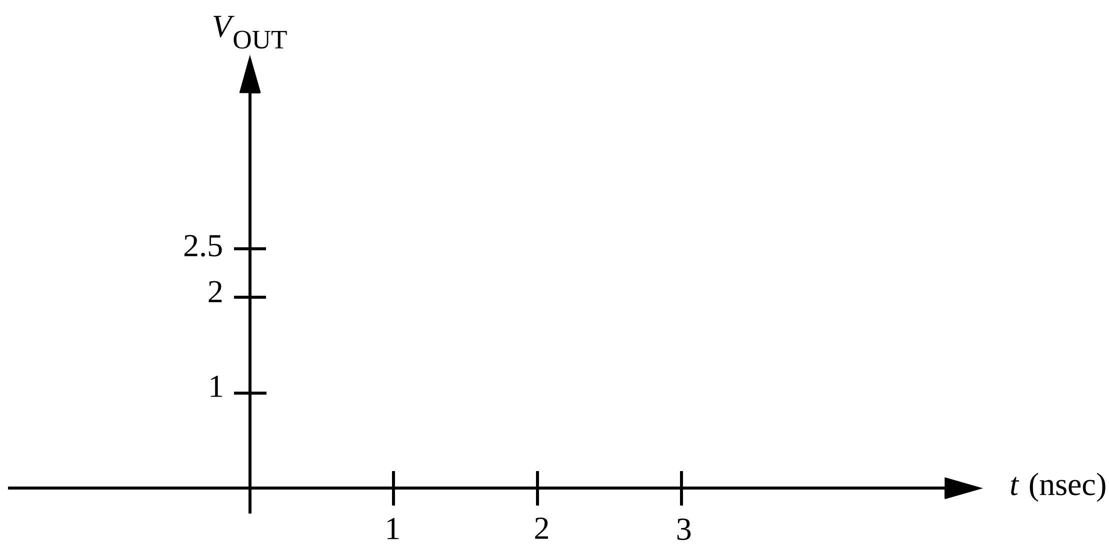
(b)

b.1) $V_{OUT}(t = 0+)$ = ______________

b.2) $V_{OUT}(t = 1\text{ nsec})$ = ______________

b.3) $V_{OUT}(t = 2\text{ nsec})$ = ______________

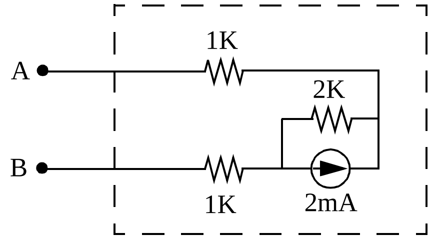
(c)



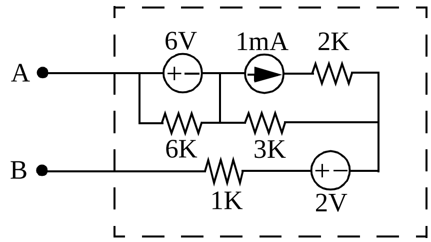
Problem 6 Thévenin Equivalents (20 points)

Find the Thévenin equivalent circuit for each of the following.

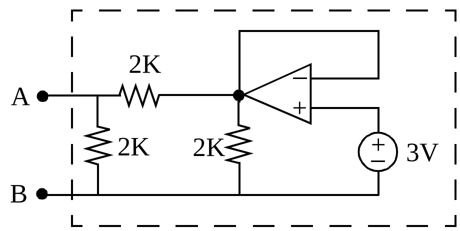
(a)



(b)

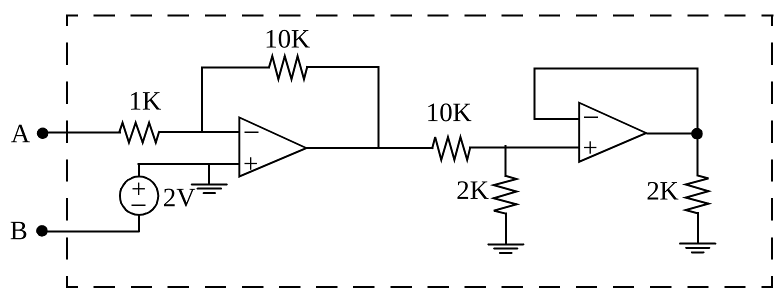


(c)



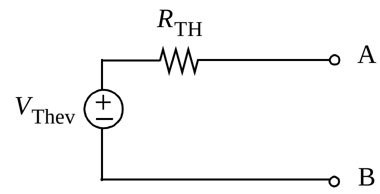
(Op-amp is ideal)

(d)



(Op-amps are ideal)

Problem 6 Worksheet and Answers



(a)

V_{TH} = ______________

R_{TH} = ______________

(b)

V_{TH} = ______________

R_{TH} = ______________

(c)

V_{TH} = ______________

R_{TH} = ______________

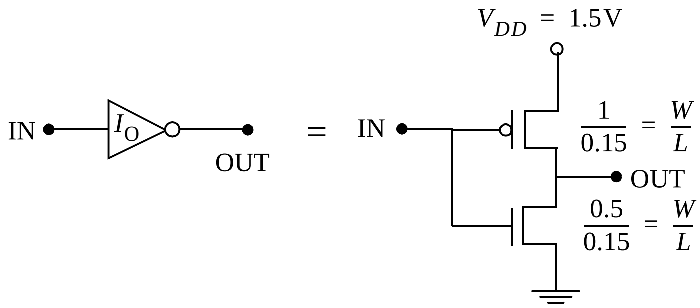
(d)

V_{TH} = ______________

R_{TH} = ______________

Problem 7 Capacitive Load (25 points)

We are designing a CMOS logic circuit with the latest devices that use $L = 0.15\mu m$. An inverter schematic is shown for the basic inverter

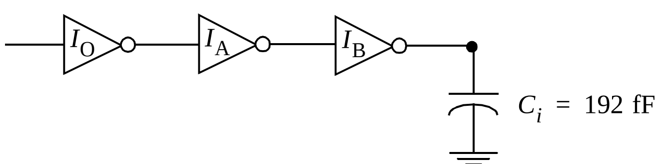


$C_{Gp} = 2fF$
$C_{Gn} = 1fF$
$R_p = 3.5K$
$R_n = 3.5K$

We need to drive an interconnect wire going across the chip with a capacitance of 192 fF.

(a) Estimate the stage delay (time to switch the output from zero to $V_{DD}/2$ with the input going from V_{DD} to 0) if this inverter drives the wire directly. The 192fF load is connected to the node labeled "OUT".

(b) Suppose we insert two "buffer inverters" that have larger W/L (and therefore, lower R_p, R_n) to drive the load capacitance faster:



For Inverter A: $\left.\frac{W}{L}\right|_N = \frac{2}{0.15}$

$\left.\frac{W}{L}\right|_P = \frac{4}{0.15}$

For Inverter B: $\left.\frac{W}{L}\right|_N = \frac{8}{0.15}$

$\left.\frac{W}{L}\right|_P = \frac{16}{0.15}$

Now we suffer 3 stage delays! But let's compute them – maybe it's not so bad. Assume the load on I_O is the gate capacitance of I_A and similarly that the load on I_A is the input capacitance of I_B.

(b.1) Compute C_{Gn} and C_{Gp} for I_A and I_B.

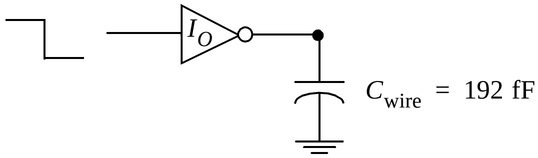
(b.2) Compute R_p and R_n for I_A and I_B.

(c-e) Find the unit gate delay for all 3 stages (input step $V_{DD} \rightarrow 0$ or 0 - V_{DD} and output moving from 0 to $V_{DD}/2$ or V_{DD} to $V_{DD}/2$).

(f) Compare total gate delay with that of part (a).

Problem 7 Worksheet and Answers

(a)

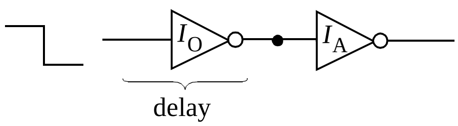


Unit gate delay = ________________ps

(b)

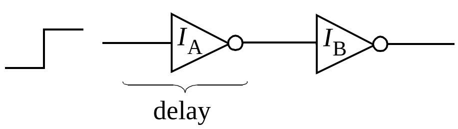
	Inverter A	Inverter B
C_{Gn}	________	________
C_{Gp}	________	________
R_p	________	________
R_n	________	________

(c)



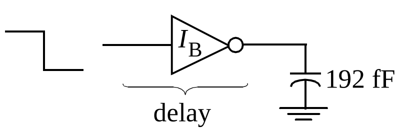
Unit gate delay = ________________

(d)



Unit gate delay = ________________

(e)

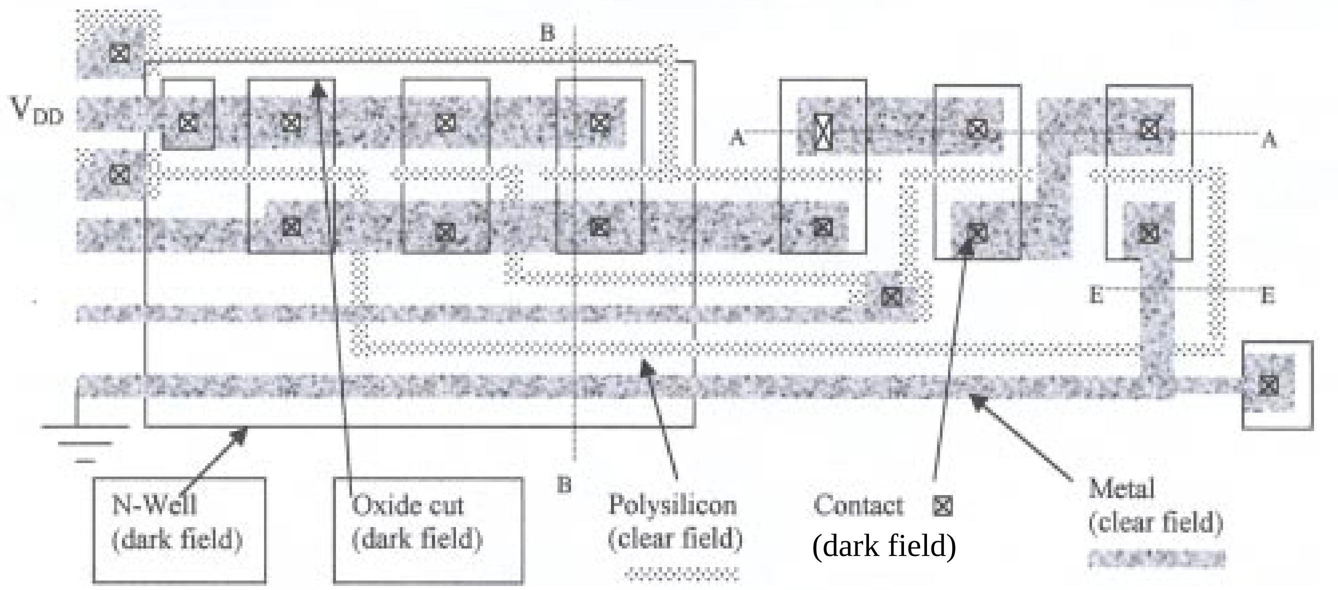


Unit gate delay = ________________

(f) Total of (c) + (d) + (e) ___________ versus (a) ___________

Problem 8 CMOS Technology (30 points)

The layout of a CMOS logic circuit is shown below. Also shown on the page opposite is the cross-section E-E of the chip.



Our standard CMOS process is:

(1) Start: p-Type Si wafer

(2) Well mask, implant donors

(3) Grow field oxide 0.5µm

(4) Pattern oxide (oxide cut for thin oxide)

(5) Grow gate oxide

(6) Deposit 0.5µm polysilicon

(7) Pattern polysilicon

(8) Two select masks with implants (masks not shown)

(9) Deposit 0.5µm oxide

(10) Contact mask, etch oxide

(11) Deposit 0.5µm metal

(12) Pattern metal

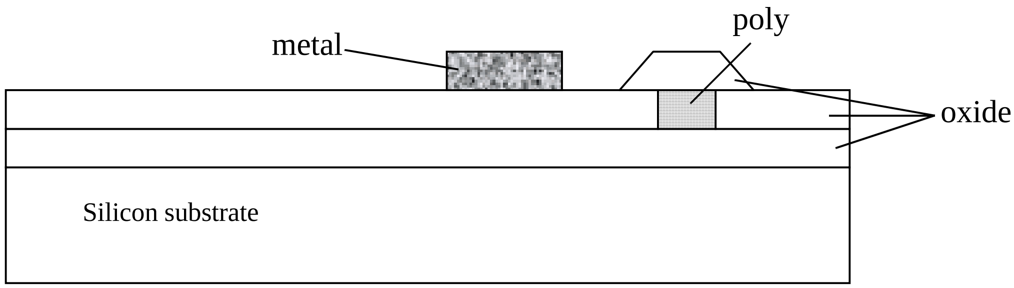
(a) In the space provided, draw cross-section A-A. Use E-E as a guide for scale.

(b) Draw cross-section B-B.

(c) Label the inputs and outputs of this circuit on the figure above. (Note that there are 6 wires entering from the left and of these, only 2 are labeled, namely V_{DD} and ground. You are to label the others and use these labels in part d.)

(d) Write the logic function of the circuit (for example, $\text{OUT} = \overline{(A+B)\cdot \overline{C}}$).

<u>Problem 8 Answers</u>



Cross-section E -- E

(a)

Cross-section A-A

(b)

Cross-section B-B

(c) (Label figure on opposite page.)

(d) Logic Equation OUT = ______________________________