University of California at Berkeley
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 Final Examination

Fall 1998 Prof. Roger T. Howe December 14, 1998

Name: _____ ***Student ID*** _____
Last, first

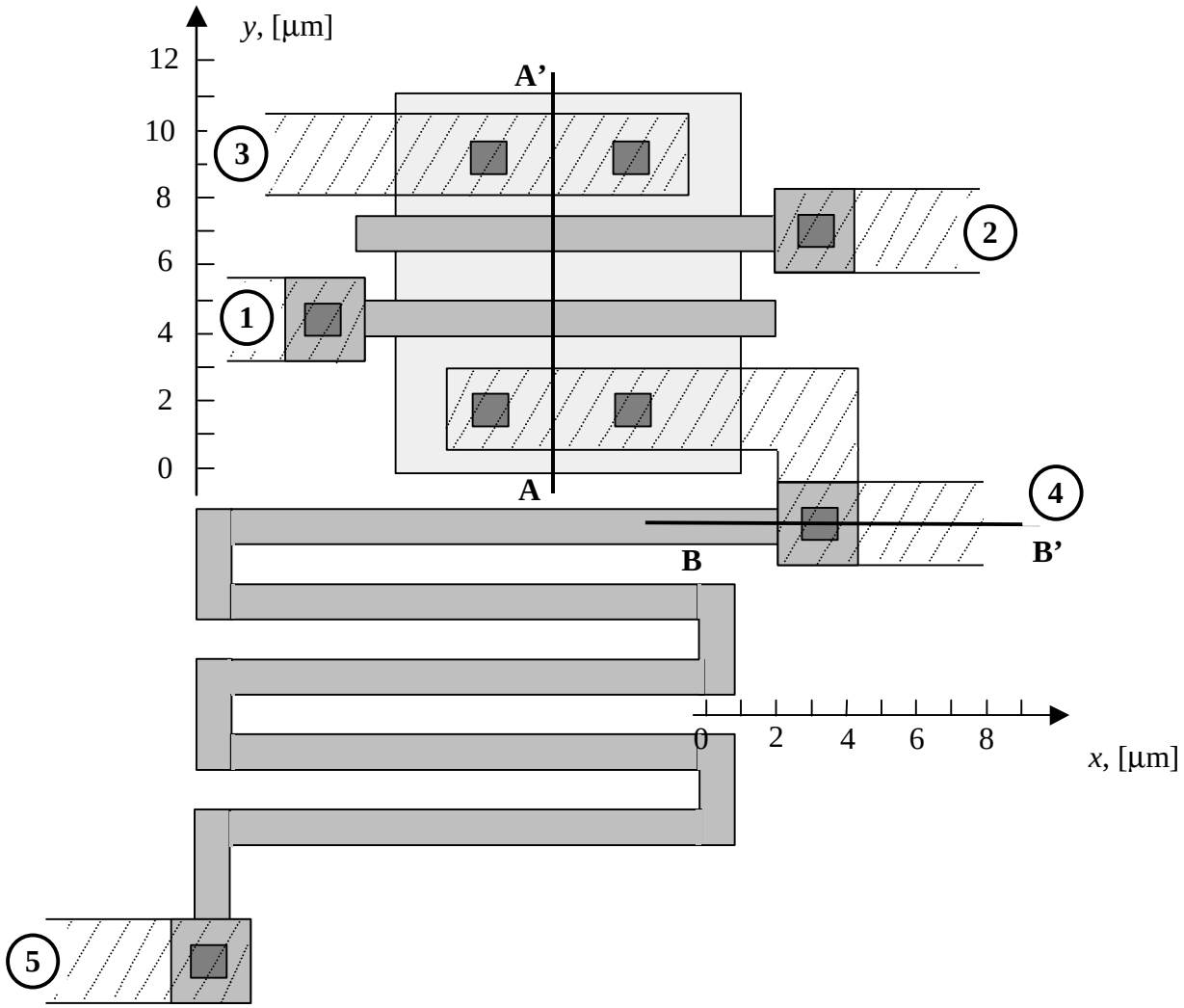
Guidelines

1. Closed book and notes; 3, 8.5" x 11" page (both sides) of your own notes are allowed.
2. You may use a calculator.
3. Do not unstaple the exam.
4. Show *all your work and reasoning on the exam* in order to receive full or partial credit.

Score

Problem	Points Possible	Score
1	25	
2	20	
3	20	
4	20	
5	15	
Total	100	

1. Digital Logic Gate [24 points]

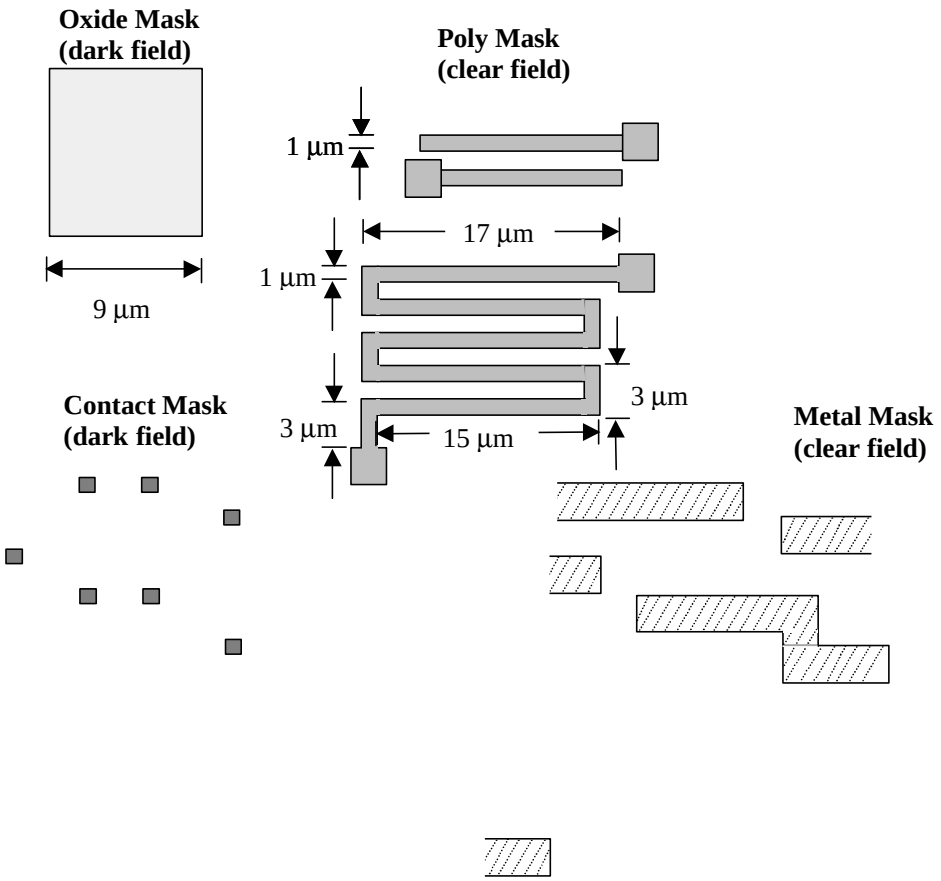


Process Sequence:

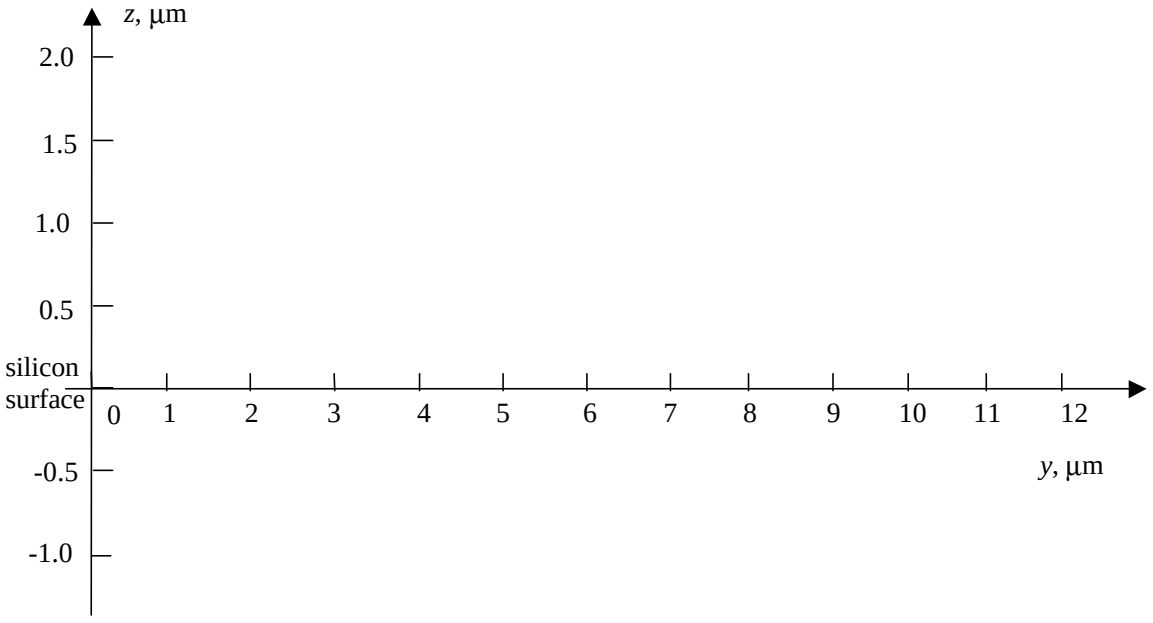
Starting material: phosphorus-doped silicon, concentration 5 x 10^{17} cm^{-3}

1. Deposit 500 nm of silicon dioxide and pattern using the **oxide mask** (dark field)
2. Grow 5 nm of thermal silicon dioxide.
3. Deposit 500 nm of boron-doped polysilicon and pattern using the **poly mask** (clear field).
4. Implant boron and anneal (depth 250 nm and concentration = 1.25 x 10^{18} cm^{-3}.)
5. Deposit 500 nm of silicon dioxide and etch 505 nm of oxide using the **contact mask** (dark field).
6. Deposit 500 nm of aluminum and pattern using the **metal mask** (clear field).

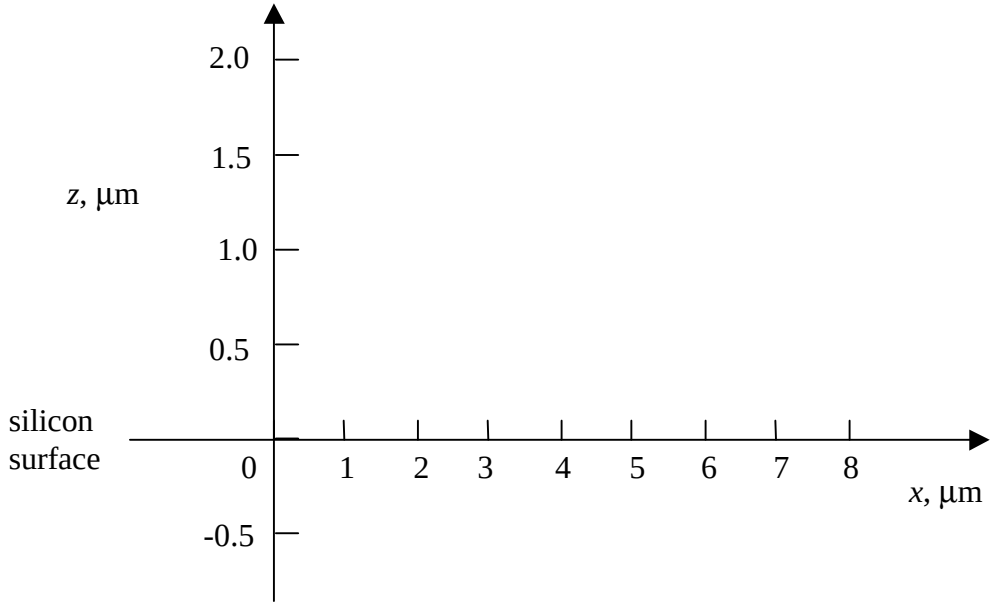
Given: polysilicon sheet resistance: R = 25 Ω/ , ε_{ox} = 3.45 x 10^{-13} F/cm,
R_{on} = 150 Ω (on resistance for MOSFET)



(a) [6 pts.] Sketch the cross section ***A-A'*** on the graph below. Identify all layers clearly.



(b) [6 pts.] Sketch the cross section ***B-B'*** on the graph below. Identify all layers clearly.



(c) [5 pts.] Given: metal lines 1-5 on the layout are connected as listed:

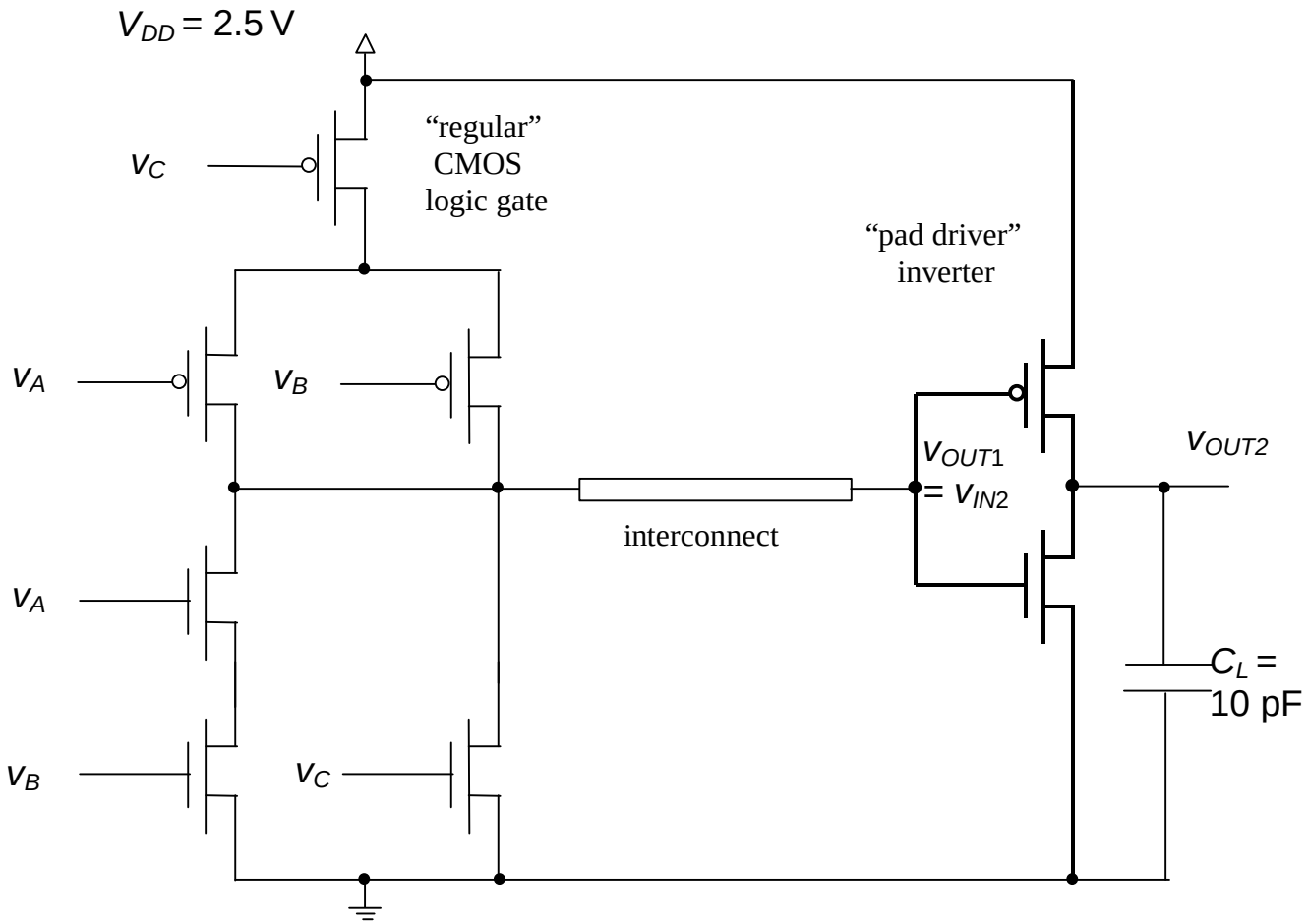
1. v_{IN1} **2**. v_{IN2} **3**. V_{DD} = 2.5 V **4**. v_{OUT} **5**. Ground.

First, draw the circuit model for the physical structures between nodes 1, 2, 3, and 4 using the correct MOSFET symbol. Second, redraw the circuit model using the "switch model" for the transistors. Give numerical values for any resistors or capacitors; you can neglect the drain-to-bulk capacitors.

(d) [4 pts] Draw the circuit model for the physical structures between nodes 4 and 5 *only*. Given: for finding the resistance, there are 70 squares of polysilicon between nodes 4 and 5. Hint: it is *not* necessary to use multiple lumps here.

(f) [4 pts.] What is the maximum value of the output voltage in Volts?

2. CMOS digital circuit [20 points]



"Regular" PMOS:
Gate capacitance: C_{ox} = 2 fF/μm^2
Width = W_p = 3 μm
Length =L_p = 0.5 μm
"on" resistance = R_p = 300 Ω

"Regular" NMOS:
Gate capacitance: C_{ox} = 2 fF/μm^2
Width = W_n = 2 μm
Length =L_n = 0.5 μm
"on" resistance = R_n = 200 Ω

V_{Th} = 1.9 V, V_{Tl} = 0.6 V

Interconnect:

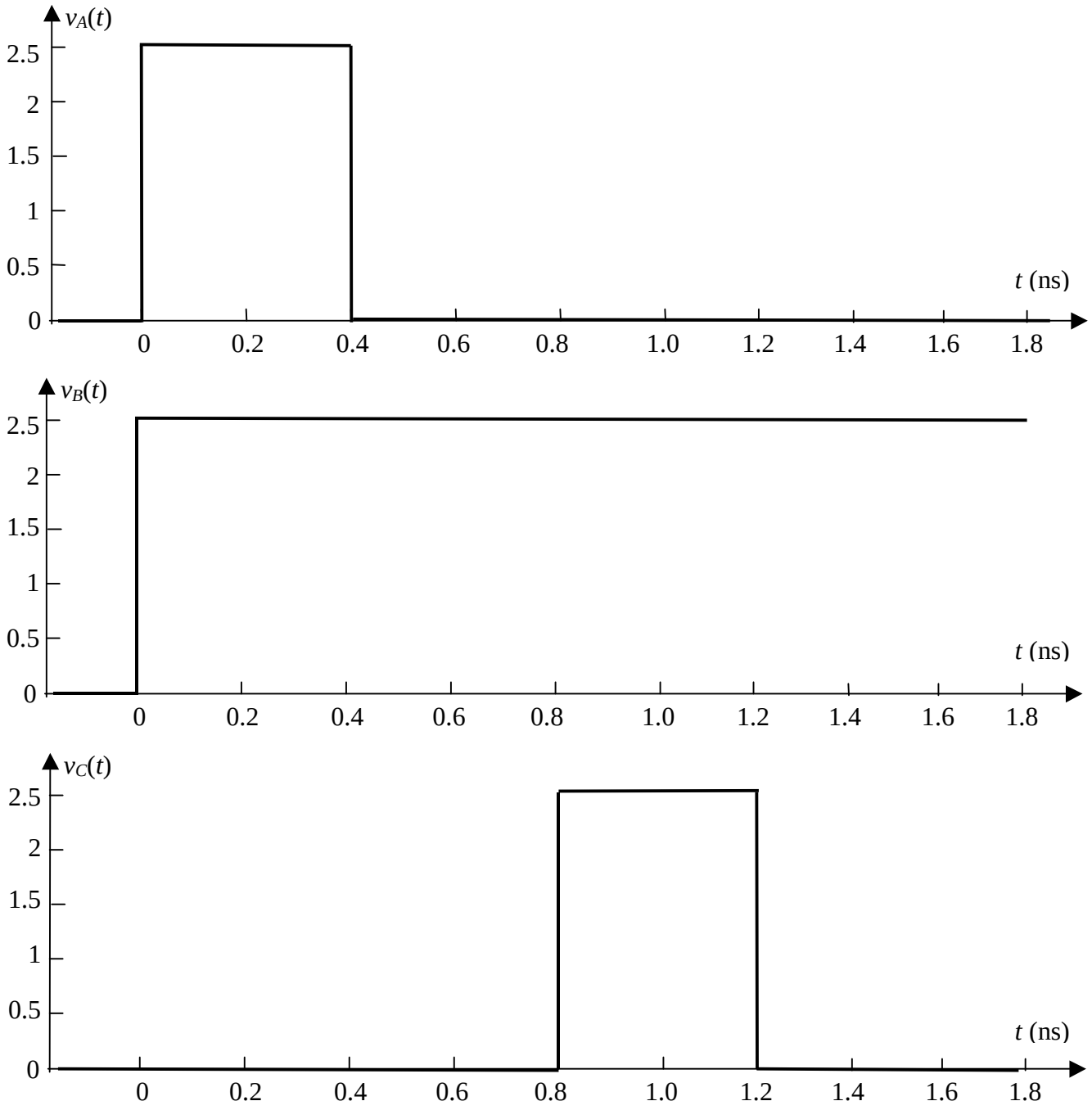
C_{int} = 0.2 fF /μm
R_{int} = 0.1 Ω /μm
L = 800 μm

"Pad Driver" PMOS:
Gate capacitance: C_{ox} = 2 fF/μm^2
Width = W_p = 150 μm
Length =L_p = 0.5 μm
"on" resistance = R_p = 15 Ω

"Pad Driver" NMOS:
Gate capacitance: C_{ox} = 2 fF/μm^2
Width = W_n = 100 μm
Length =L_n = 0.5 μm
"on" resistance = R_n = 10 Ω

V_{Th} = 1.4 V, V_{Tl} = 1.1 V

The waveforms for $v_A(t)$, $v_B(t)$, and $v_C(t)$ are:



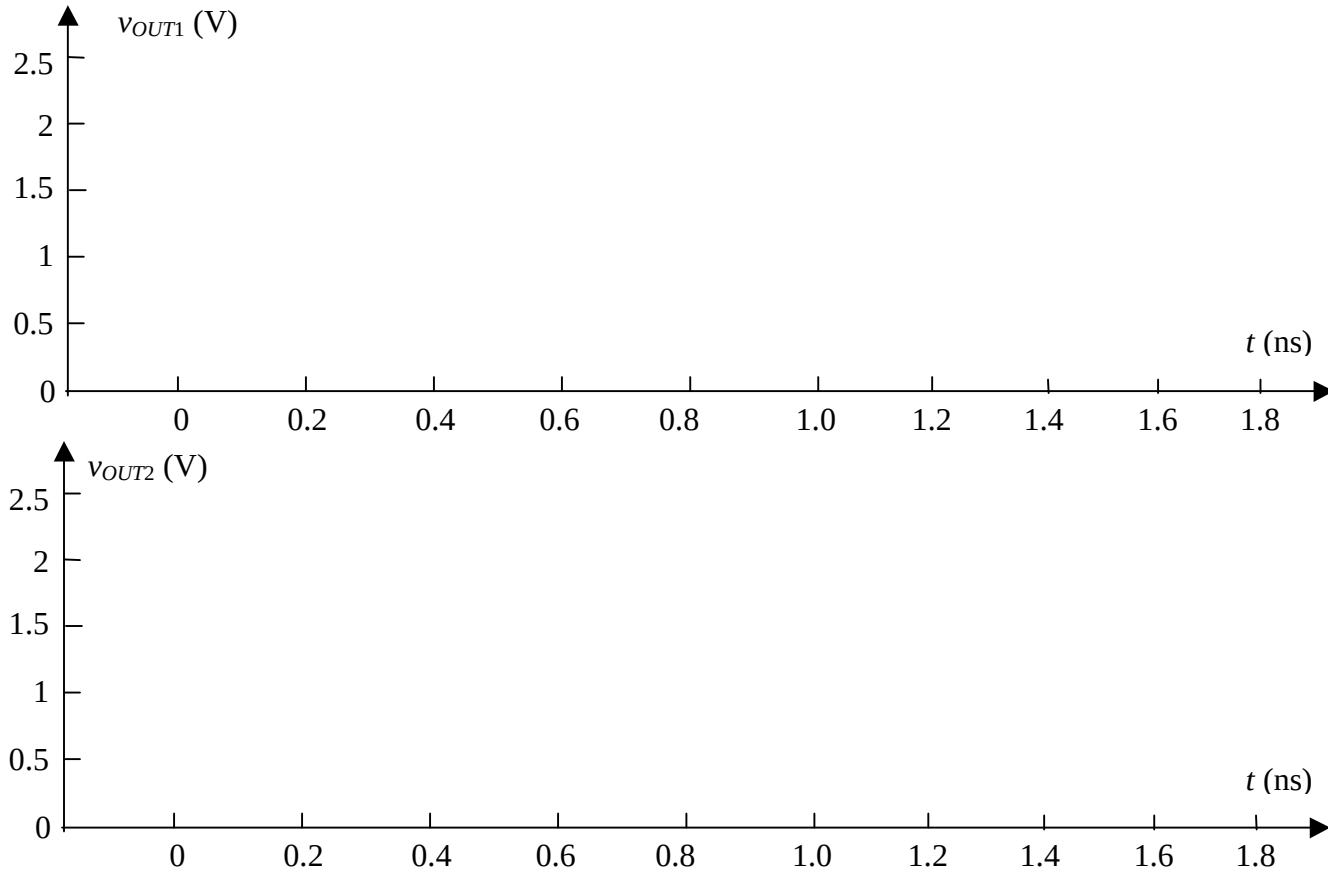
(a) [2 pts.] The input voltages to this circuit have been constant for a long time for $t < 0$. What are the numerical values of the voltages v_{OUT1} and v_{OUT2} for $t < 0$?

(b) [4 pts.] Find the waveform $\boldsymbol{v_{OUT1}(t)}$ for the time interval $0 < t < 0.4$ ns.

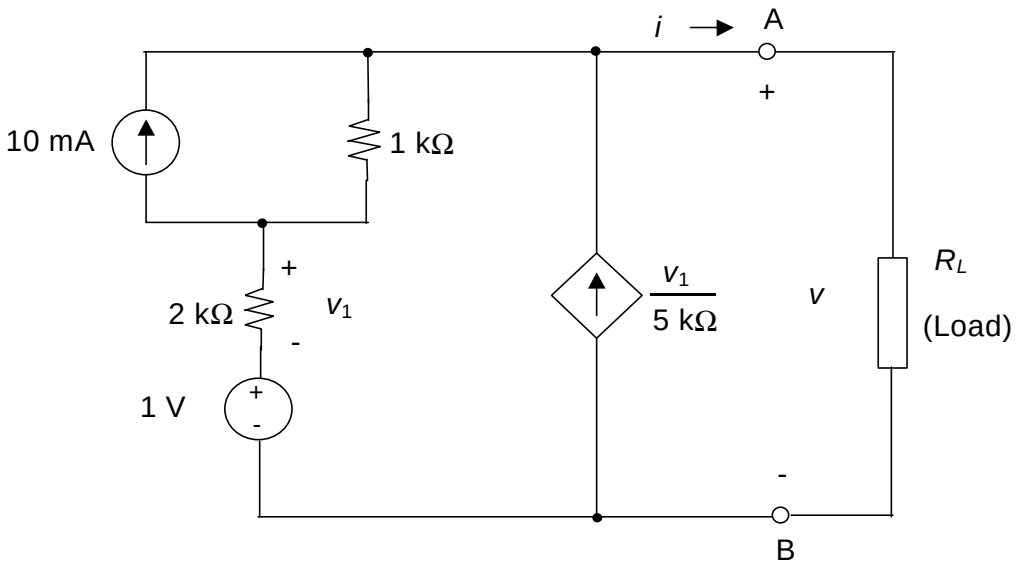
(c) [4 pts.] Find the waveform $\boldsymbol{v_{OUT2}(t)}$ for the time interval $0 < t < 0.4$ ns.

(d) [4 pts.] Find the waveform $\boldsymbol{v_{OUT1}(t)}$ for the time interval $0.4 < t < 0.8$ ns. If you couldn't solve part (b), you can assume for this part that $\boldsymbol{v_{OUT1}}(0.8\text{ ns}) = 2.5$ V.

(e) [6 pts.] Sketch the waveforms $v_{OUT1}(t)$ and $v_{OUT2}(t)$ on the graphs below over the interval $0 < t < 1.8$ ns. Note that the logic thresholds for the pad driver are different from those of the regular CMOS logic gate. Your sketch should be consistent with your answers for (a) – (d).



3. Linear circuit analysis [20 points]

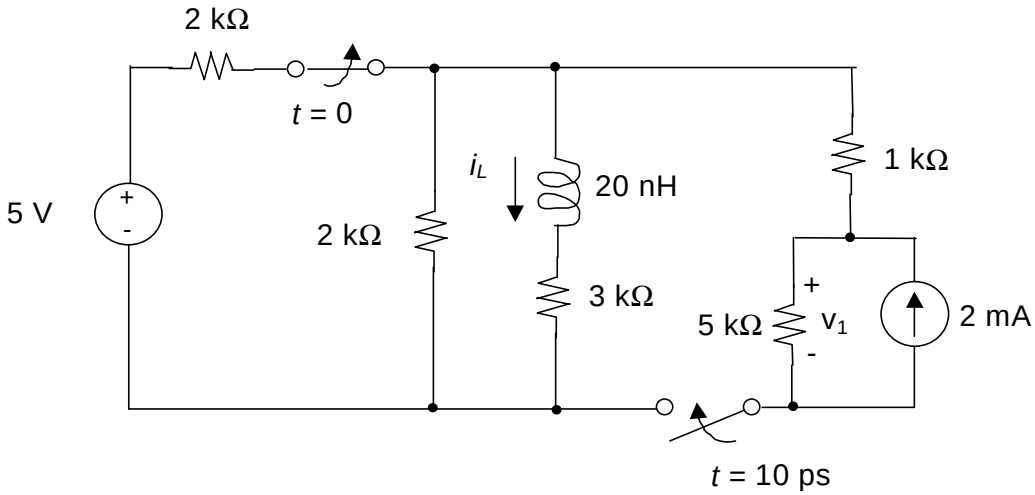


(a) [8 pts.] What is the numerical value of the Norton equivalent current I_N for this two-terminal linear network?

(b) [8 pts.] What is the numerical value of the Thevenin equivalent resistance R_{Th} for this two-terminal linear network?

(c) [4 pts.] What is the numerical value of the maximum power that can be extracted from this two-terminal network in Watts? What is the numerical value of the load resistance R_L required for this case? If you couldn't solve parts (a) and (b), you can assume for this part that I_N = 20 mA and R_{Th} = 8 kΩ.

4. Inductor-resistor circuit analysis [20 points]



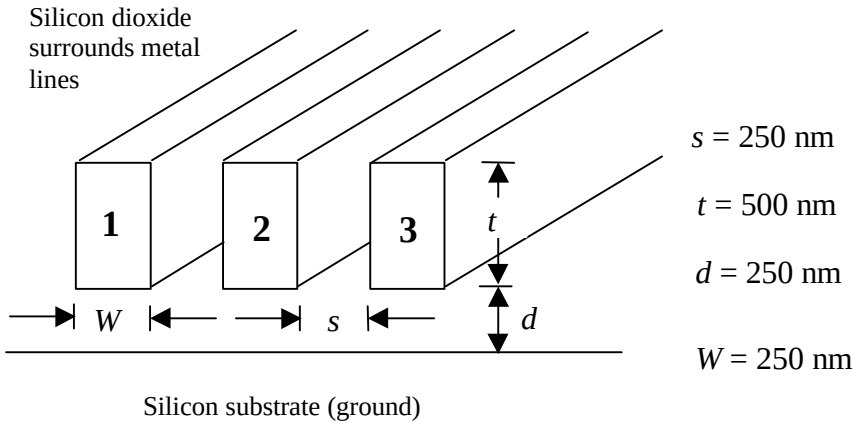
(a) [4 pts.] What is the numerical value of the inductor current $i_L(0)$ when $t = 0$.

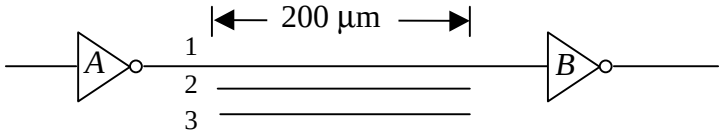
(b) [4 pts.] Find the numerical value of the final inductor current, $i_L(t \to \infty)$.

(c) [6 pts.] Find the inductor current $i_L(t)$ for $0 \le t \le 10\,ps$.

(d) [6 pts.] Find the inductor current $i_L(t)$ for $t \ge 10\,ps$.

5. Capacitive coupling [15 points]





Inverters A and B: $R_n = R_p = 100\ \Omega$ $V_{DD} = 2.5$ V

$C_{Gn} + C_{Gp} = 25$ fF

The interconnect (line 1) between inverters *A* and *B* runs close by lines 2 and 3, as shown in the cross section, for a distance of 200 μm. The interconnects are surrounded by SiO_2. Lines 2 and 3 are floating (not connected to anything at either end).

(a) [5 pts.] Draw the circuit model for the pull-up transition of inverter *A*. Include the numerical values of the capacitors between lines 1, 2, and 3 (and between them and the grounded substrate); you can neglect the interconnect resistance.
Given: $\varepsilon_{ox} = 3.45 \times 10^{-13}$ F/cm.

(b) [5 pts.] Find the peak voltage $v_{2,\max}$ on line 2 after the pull-up transition of inverter *A*.

(c) [5 pts.] Find the peak voltage $v_{3,\max}$ on line 3 after the pull-up transition of inverter *A*.