# EECS 40, Fall 2009
# Midterm Exam #2

Nov 5, 2009
Total Time Allotted: 80 minutes

***DO ALL WORK ON EXAM PAGES***
***(Exam paper has a total of 9 pages including cover page)***

1. Closed book exam. You are allowed to bring two sheets (8.5" x 11") of notes.
2. You can use a calculator. NO cell phone or computer.
3. If you put down the wrong answer, partial credits will be given only if you show the correct steps.
4. Points will be taken off for answers without units.

Last (Family) Name:____**Solutions**_____

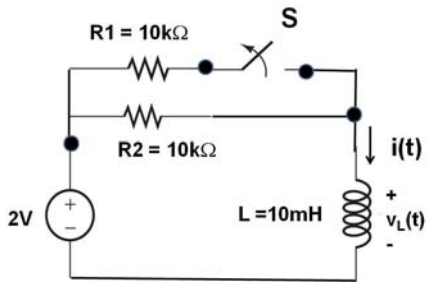
First Name: _____

Student ID: _____Discussion Session (# or TA): _____

Signature: _____

| | |
|---|---|
| **Problem 1 (20 points)** | |
| **Problem 2 (20 Points)** | |
| **Problem 3 (25 Points)** | |
| **Problem 4 (9 Points)** | |
| **Problem 5 (6 points)** | |
| **Problem 6 (10 Points)** | |
| **Problem 7 (10 Points)** | |
| **TOTAL (100 points)** | |

## Problem 1 First-order Circuit Transient (20 points total)




(a) (3 points) For time t <0, the switch **S** is closed and the circuit is at steady state. What is the value of current i?

For t<0, inductor is a short.

**i**= 2V/(10kΩ/2) = **0.4 mA**

(b) (5 points) The switch S is opened at t= 0, determine the i(t) expression for t>0 and the time constant

i(t) = A + B•exp(-t/τ) and i(t) through inductor is continuous with t.

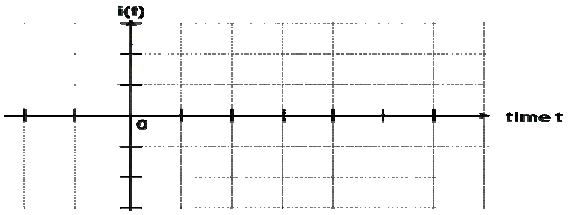
**τ = 10mH/10kΩ= 1 μsec**

i(0)=0.4mA

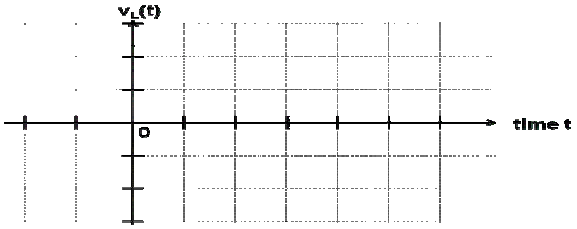
i(+∞) =2V/(10kΩ) = 0.2 mA

**A=0.2mA, B=0.2mA**

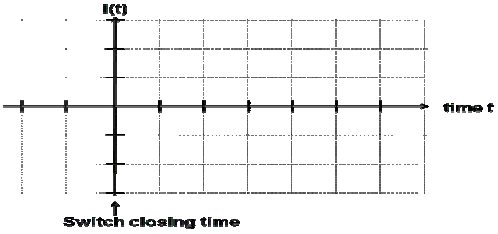
(c) (4 points) Sketch i(t) for all t in the graph paper provided below. Label time scale, initial value, and asymptotic value.



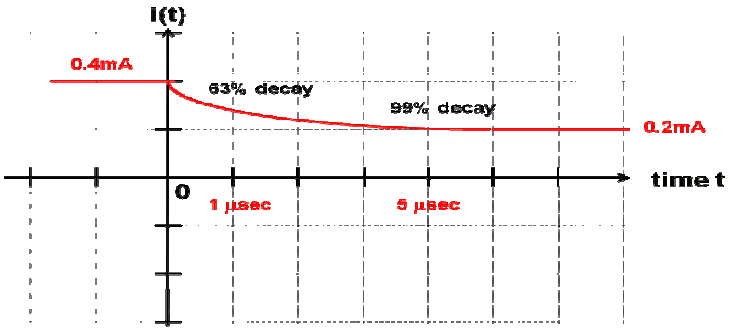

(d) (3 points) Sketch the voltage across the inductor $v_L(t)$ for all t in the graph paper provided below. Label time scale, initial value, and asymptotic value.




(e) (5 points) After the switch S has been opened for a long time (i.e. new steady state), it is closed again. (i) Sketch i(t) after this switching. Label time scale, initial value and asymptotic value. (ii) Calculate the value of the new time constant .



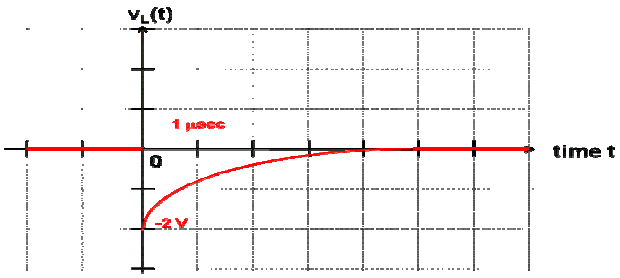
**Ans**

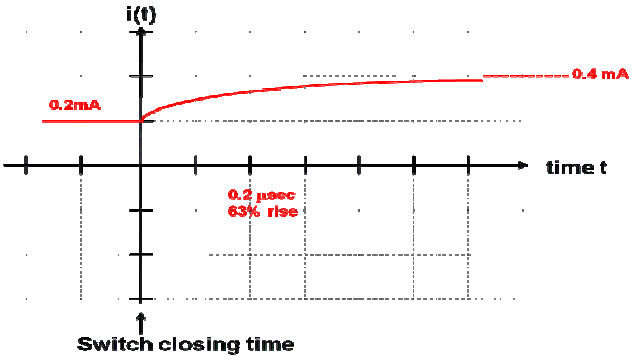



$v_L(t) = L \bullet di/dt$

$= - (10mH \bullet 2 \bullet 10^{-4}\ Amp/10^{-6}\ sec) \bullet exp(-t/1\mu sec)$

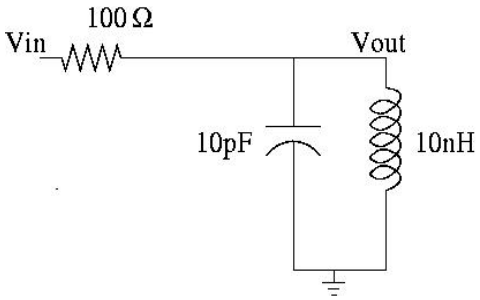
$= -2V \bullet exp(-t/1\mu sec)$




**$\tau$ (new)= 10mH/(10kΩ/2)= 2 µsec**

**Problem 2 Resonance (20 points total)**




For this circuit

a) (5 points) Derive expression for the phasor ratio: $\mathbf{V}_{out}/\mathbf{V}_{in}$

$\mathbf{V}_{out}/\mathbf{V}_{in} = j\,w\,L/R * 1/(1-w^2LC+j\,w\,L/R) = j\,(w/w_0\,Q)\,/[1-(w/w_0)^2 + j\,w/(w_0\,Q)]$

b) (5 points) Calculate the center frequency $f_0$ [Measured in Hz]

c) $\omega_0 = \mathrm{sqrt}(LC)^{-1}$

f0 = 500 MHz

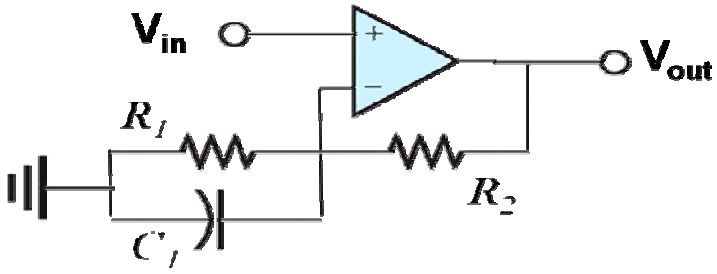
(5 points) Calculate the 3dB bandwidth BW

Q=sqrt(C/L)*R = 3.16
BW = fo/Q = 160 MHz

d) (5 points) Indicate new component values for the capacitor and the inductor if the filter center frequency and the bandwidth have to be decreased by a factor of 10. R is kept constant [Hint: try to keep the filter Q constant]

To decrease center frequency without changing Q, change L and C such that their ratio is constant:
C'=10C=100pF;
L'=10L=100nH

**Problem 2 Active filter (25 points total)**




Assume an ideal op amp. Given:

$$R_1 = 1\ \text{k}\Omega, \qquad R_2 = 10\ \text{k}\Omega, \qquad C_1 = 1\ \text{nF}$$

a) (5 points) What type of filter is this? You should be able to determine this with no calculations.

Highpass

b) (5 points) Calculate the DC gain in dB.

Use the formula for a noninverting amplifier:

$$H(f) = 1 + \frac{R_2}{R_1 || C_1}$$

$$= 1 + \frac{R_2}{\frac{R_1}{1 + j\omega R_1 C_1}}$$

$$= 1 + \frac{R_2(1 + j\omega R_1 C_1)}{R_1}$$

$$= 1 + \frac{R_2}{R_1} + j\omega R_2 C_1$$

$$= \left(1 + \frac{R_2}{R_1}\right) \cdot (1 + j\omega (R_2 || R_1) C_1)$$

Identify the DC gain:

$$H_{DC} = 1 + \frac{R_2}{R_1}$$

$$= 11 = 20.8 \text{ dB}$$

c) (5 points) Calculate all break frequencies and identify as pole or zero.

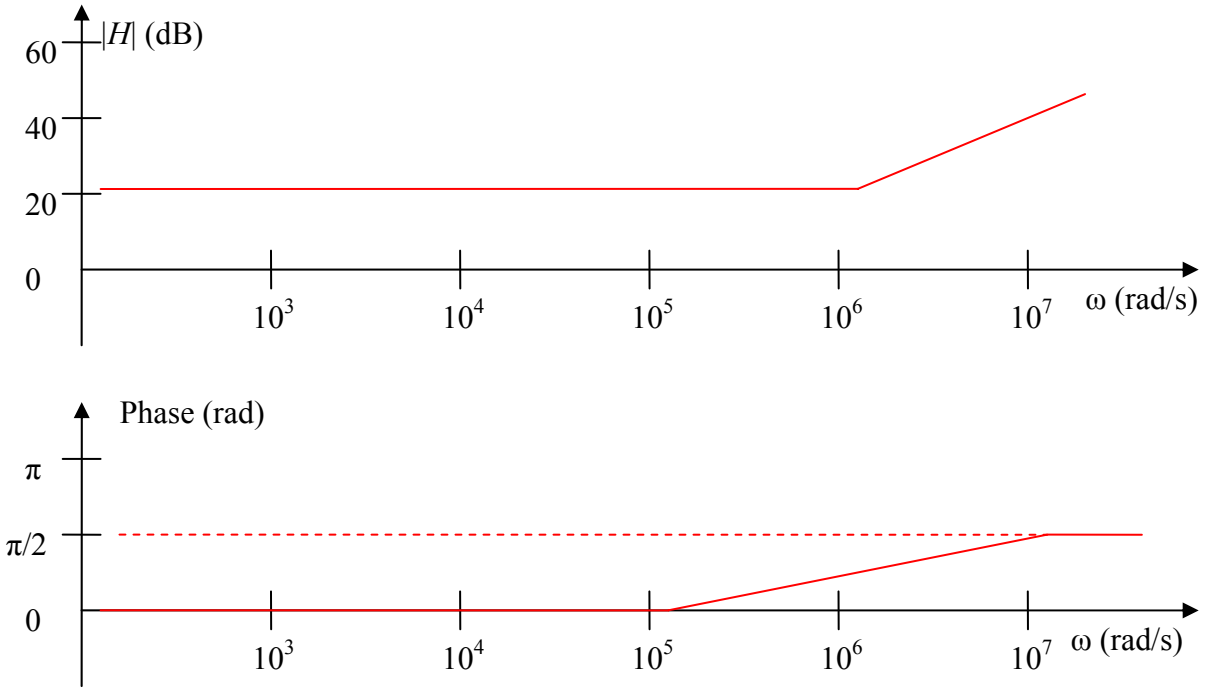
Identify the zero frequency from the above expression for *H*:

$$\omega_z = \frac{1}{(R_2 || R_1) C_1}$$

$$= 1.10 \frac{\text{Mrad}}{\text{s}}$$

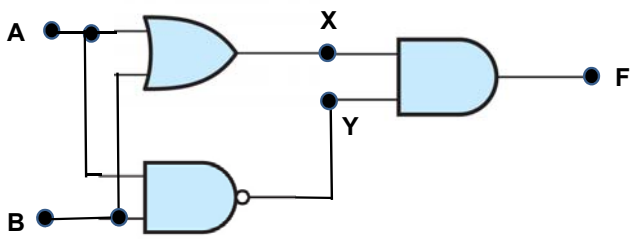
**Problem 3 continued**

(10 points) Sketch the Bode magnitude and phase plots.



## Problem 4 Logic Gate, Truth Table and Boolean Algebra (9 points)

A logic gate circuit is shown below




a) (3 points) Write the Boolean logic expression of output **F**

$$F = (A + B)(\overline{AB})$$

b) (3 points) Fill in the missing truth table entries of the circuit:

| A | B | X | Y | F |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |

c) (3 points) From the truth table, write the minimal sum of products form of **F**

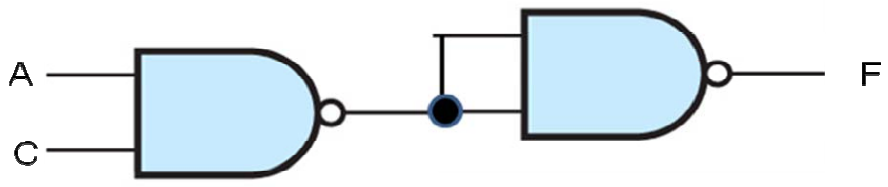
$$F = A\overline{B} + \overline{A}B$$

**Problem 5 Boolean algebra and gate implementation (6 points)**

(a) (3 points) Use Boolean algebra to simply the expression F=(A+AB)C(C+D) such that F can be implemented with ***only two 2-input NAND gates***.

$$F = A(1+B)(CC+CD) = A(C+CD) = AC(1+D) = AC = \overline{\overline{AC}}$$

(b) (3 points) Sketch the 2 NAND gate circuit diagram.



**Problem 6 Karnaugh Map and SOP (10 points)**

Below is shown the truth-table of a 4 variable logic function F. "X" denotes "don't care".

A B C D F
0 0 0 0 X
0 0 0 1 1
0 0 1 1 0
0 0 1 0 0
0 1 1 0 0
0 1 0 0 1
0 1 0 1 X
0 1 1 1 0
1 1 1 1 X
1 1 1 0 0
1 1 0 0 0
1 1 0 1 0
1 0 0 1 0
1 0 0 0 0
1 0 1 0 X
1 0 1 1 0The
Karnaugh Map is shown below.

| AB\CD | 0 0 | 0 1 | 1 1 | 1 0 |
|---|---|---|---|---|
| **0 0** | **X** | **1** | **0** | **0** |
| **0 1** | **1** | **X** | **0** | **0** |
| **1 1** | **0** | **0** | **X** | **0** |
| **1 0** | **0** | **X** | **0** | **X** |

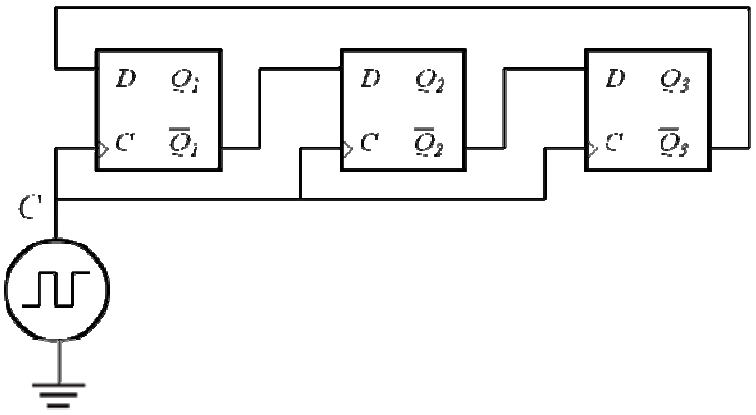
a) (6 points) Replace the "X" boxes with either "1" or ")" so your SOP implementation uses the **fewest gates**. You are allowed only to use NOT, AND,and OR gates.

| AB\CD | 0 0 | 0 1 | 1 1 | 1 0 |
|---|---|---|---|---|
| 0 0 | X (1) | 1 | 0 | 0 |
| 0 1 | 1 | X (1) | 0 | 0 |
| 1 1 | 0 | 0 | X (0) | 0 |
| 1 0 | 0 | X(0) | 0 | X (0) |

b) (4 points) Write the Boolean expression of your SOP implementation

$\overline{A}\,\overline{C}$

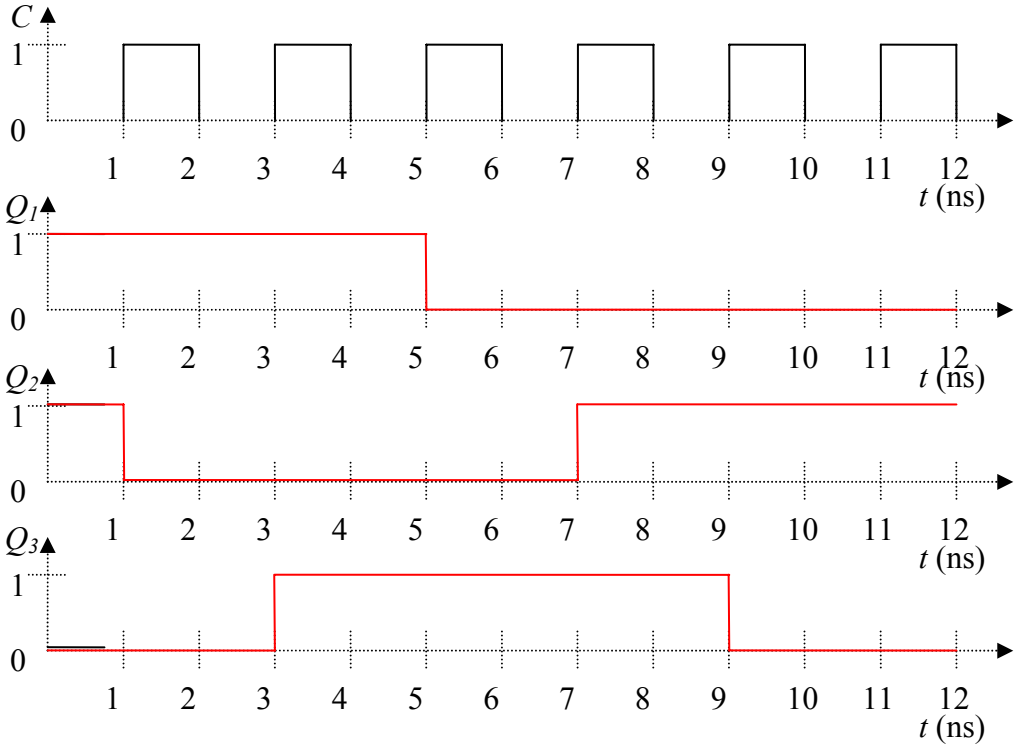
## Problem 7 Sequential logic (10 points)




In the circuit above, the flip-flops are positive-triggered *D* flip-flops. The truth table is repeated for your convenience.
The logic value of the clock signal *C* and the initial logic values of the three stored variables $Q_n$ are shown on the timing diagrams. ($Q_1(0) = 1$, $Q_2(0) = 1$, $Q_3(0) = 0$)

| *C* | *D* | *Q* |
|---|---|---|
| 0 | x | $Q_{n-1}$ |
| 1 | x | $Q_{n-1}$ |
| ↑ | 0 | 0 |
| ↑ | 1 | 1 |

a) Fill in the remaining timing diagrams through $t$ = 12 ns. (7 pts)




b) What are the periods of the clock (*T*) and *Q* signals ($T_n$)? Give correct units. (3 pts)

$T = 2$ ns, $T_n = 12$ ns