## EE 40 Midterm 3

## Fall 2002

## Problem 1: 10 Points

Fill in the blanks to correctly complete the sentences.
To improve conduction in silicon, atoms from other elements are incorporated into the lattice.
The addition of Group III elements creates $\qquad$ - type material.

For example, $\qquad$ is a Group III element that might be added to the silicon.

The addition of Group V elements creates $\qquad$ - type material.

For example, $\qquad$ is a Group V element that might be added to the silicon.

The Group $\qquad$ elements need one more electron in the outer shell to complete all four lattice bonds.

This lack of an electron is called a $\qquad$ .

When the two types of material are joined together, electrons cross the junction between the two materials to complete lattice bonds where needed.

The movement of free electrons from an area of greater concentration to lesser concentration, motivated by the need to complete lattice bonds, is called $\qquad$
This creates a layer without free charge carriers, called the $\qquad$ layer.

The movement of electrons creates positive charge in the atoms the electrons have left behind, and negative charge in the atoms which the electrons have joined. This creates a potential difference across the junction; the $\qquad$ - type material is at a higher potential.

This causes electrons to move across the junction towards the higher electric potential. This movement, due to attraction by positive potential, is called $\qquad$ .

Problem 2: 20 Points
Determine the logical operation performed by the circuit below:


## Problem 3: 10 Points

Consider the following circuit, with the input voltage just below $\mathrm{V}_{\mathrm{dd}}-\mathrm{V}_{\text {т. }}$ Here, the NMOS threshold voltage is $-\mathrm{V}_{\mathrm{T}} . \mathrm{V}_{\mathrm{T}}$ is positive, and much smaller than $\mathrm{V}_{\mathrm{DD}}$. Assume that the transistors have matched ID/VDS characteristics.

Determine the most likely mode of operation for each transistor.

## $V_{D D}-V_{T}-\varepsilon$ <br> 

Problem 4: 20 Points
Consider the following circuit. Find Vout when Vin is 3.7 V .
NMOS:
$\mathrm{V}_{\mathrm{T}(\mathrm{N})}=1 \mathrm{~V}$
lambda $=0$
$\operatorname{IdSat}_{(\mathrm{N})}=10^{-3}\left(\mathrm{~V}_{\mathrm{GS}(\mathrm{N})}-\mathrm{V}_{\mathrm{t}(\mathrm{N})}\right)^{2} \mathrm{~A}$
PMOS:
$\mathrm{V}_{\mathrm{T}(\mathrm{P})}=-1 \mathrm{~V}$
lambda $=0$
$\operatorname{IdSAT}(\mathrm{P})=10^{-3}\left(\mathrm{~V}_{\mathrm{GS}(\mathrm{P})}-\mathrm{V}_{\mathrm{T}(\mathrm{P})}\right)^{2} \mathrm{~A}$


Problem 5: 20 Points
Consider the following circuit. Find Vout when Vin is 3.7 V .
NMOS:
$\mathrm{V}_{\mathrm{T}(\mathrm{N})}=1 \mathrm{~V}$
lambda $=0$
$\operatorname{IdsAT}(\mathrm{N})=10^{-3}\left(\mathrm{~V}_{\mathrm{GS}(\mathrm{N})}-\mathrm{V}_{\mathrm{T}(\mathrm{N})}\right)^{2} \mathrm{~A}$
PMOS:
$\mathrm{V}_{\mathrm{T}(\mathrm{P})}=-1 \mathrm{~V}$
lambda $=0$
$\left.\operatorname{IdSAT}(\mathrm{P})=10^{-3}\left(\mathrm{VGS}_{\mathrm{P}} \mathrm{P}\right)-\mathrm{V}_{\mathrm{T}(\mathrm{P})}\right)^{2} \mathrm{~A}$


Problem 6: 20 Points
Sketch $\operatorname{Vout}(\mathrm{t})$ for the diode circuit
a) using the ideal model
b) using the large-signal model
c) using the small-signal model.

Provide enough detail to completely indicate the effect created by the circuit.


