UNIVERSITY OF CALIFORNIA
College of Engineering
Electrical Engineering and Computer Sciences Department

145M Microcomputer Interfacing Lab

Final Exam Solutions May 20, 1991

1A **Glitch** (of a D/A converter) Brief erroneous spike that occurs in the output of a D/A converter when >1 input bits change at slightly different times. [Note: the critical element here is that the bits change at different times- the statement that more than one bit changes was insufficient]

1B **Handshaking** (between any sender and receiver): Communication procedures used to ensure that both sender and receiver are ready before the transaction and that the data have been successfully transferred. For full handshaking the four steps are: the sender is ready, the receiver is ready, the data have been asserted, the data have been taken. [Note: the last two steps were good for full credit]

1C **Frequency Aliasing:** Erroneous lower frequencies that arise when a waveform is periodically sampled at less than twice its maximum frequency. [3 points off if answer was "one-half" rather than "twice"] [4 points off if sampling frequency not mentioned]

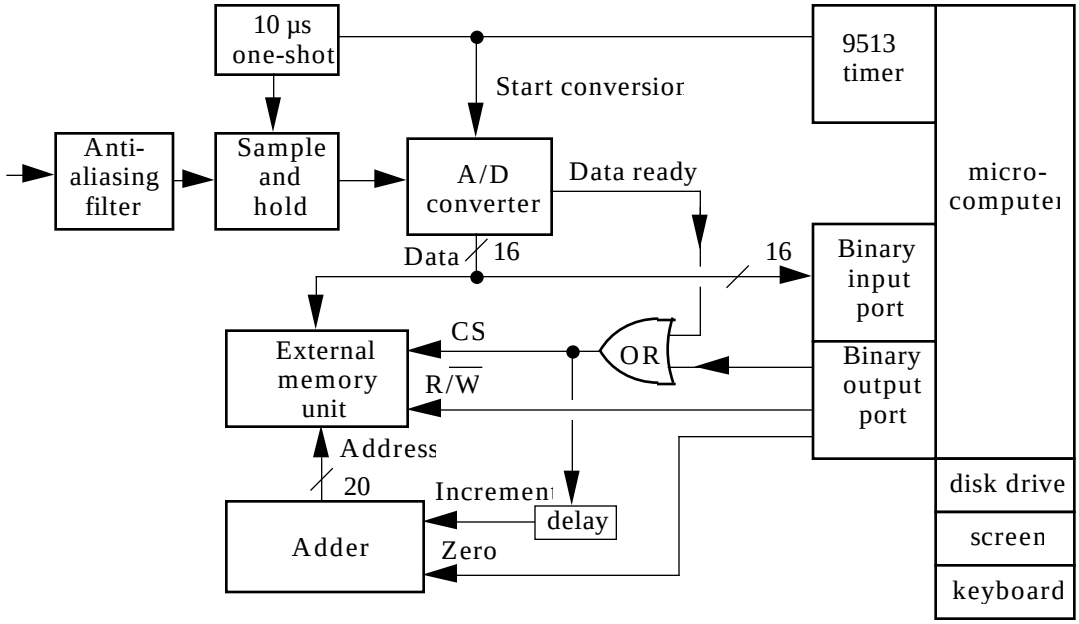
1D **Sample and Hold Amplifier:** Analog device that either amplifies an input signal or holds its output at a constant value, depending on a digital control signal. [2 points off if sample mode not mentioned]

1E **Settling time** (of a D/A converter): The time required for the output of the converter to reach its final value (within a specified error band) after a large change in the input.

1F **Two's Complement** (the operation): Procedure for complementing all the bits of an number and adding one. Adding the two's complement of a number produces the same result as subtracting the number.

1G **Formants of Vowels:** Resonance peaks in the FFT frequency spectrum (amplitude vs. frequency) determined in part by the shape of the oral cavity.

2A



[2 points off if sample-and-hold control not shown]
[5 points off if computer is in data acquisition loop]

2B PROGRAM:

1 ask for N, T, file name
2 set R/ $\overline{W}$ low for writing to external memory unit
3 clear adder
4 setup_go(T,N)
5 wait until counter(2) equals zero
6 set R/ $\overline{W}$ high for reading from external memory unit
7 clear adder
8 open file
9 use binary output to pulse external memory unit CS
10 read data lines of external memory unit into binary input port (transparent mode)
11 write data to file
12 increment adder with delayed CS pulse
13 loop back to step 9 N times

EXTERNAL CIRCUIT (actions during program step 5 – data acquisition):

1 9513 timer pulse starts 10 µs one-shot which puts S/H into hold mode
2 9513 timer pulse starts A/D conversion
3 At end of conversion, A/D converter Data Ready pulse writes data into external memory via CS line
4 After short delay, the Data Ready pulse increments the adder

EXTERNAL CIRCUIT (actions during program steps 9-13 – data retrieval)

1 binary output reads external memory unit via CS pulse
2 external memory unit data lines are read into binary input port
3 after a short delay, adder is incremented

[4 points off if external circuit function not described]

2C f_{max} = 100 kHz (limited by 10 µs A/D conversion time. f_{min} = 1 MHz/2^{32}= 1/4000 s = 250 µHz.

2D $N_{max} = 1.05 \times 10^6$ (limited by memory size). T = 10.5 s.

2E 1 step size (average) = 20 V/2^{16} = 305 µV. Specification is that individual steps are 1 LSB ± 4 LSB and could vary from –3 to +5 LSB. The answer that the step sizes could be in error by as much as 1.22 mV was accepted.

2F A low-pass filter with a sharp cut-off just below 500 Hz.

3A

1 Remove frequency components above 1/2 the sampling frequency with a low-pass filter
2 Trigger A/D converter, sample analog input, and store converted output x_j
3 Perform the digital filter operation $y_i = \Sigma A_j x_{i-j} + \Sigma B_j y_{i-j}$
4 Convert the result with a D/A converter – this is the analog output

3B

1 set up microphone and amplifier
2 use anti-aliasing filter (low pass with cut-off at about 20 kHz)
3 sample voice signal at about 40-60 kHz
4 store data in memory
5 output data to D/A at the same rate as sampled
6 amplify output for speaker

[1 point off if no microphone or amplifier]
[2 points off if no microphone, amplifier, or speaker]
[3 points off if no microphone, amplifier, or anti-alias filter]
[4 points off if no microphone, amplifier, anti-alias filter, output amp, or speaker]

3C

1 zero the digital timer
2 start the FFT
3 when the FFT is finished, read the timer
4 convert the timer count to suitable time units

Note: this procedure could be used to time any process

4A (2 kHz) (25th harmonic) = 100 kHz [3 points off for 4 kHz]

4B 10 s

4C 10^6 samples

4D $4000 \approx 2^{12}$ 12 bit accuracy required

4E Since the highest signal frequency of interest is 50 kHz (the 25th harmonic) we need a filter that passes all frequencies accurately below 50 kHz. A low pass filter with a sharp cut-off (8 poles) at 60 kHz is good, but then it is necessary to sample somewhat higher than 120 kHz to avoid aliasing. [3 points off if cutoff frequency or number of poles is not mentioned]

4F Multiply by a time window that reduces the FFT input to zero at the beginning and end of the sampling period.

4G nonzero: F_{1000} and $F_{999,000}$.

4H F_{1000}, F_{1001}, $F_{998,999}$, and $F_{999,000}$ all have the same size. Some leakage into neighboring coefficients.

4I As 4H but leakage into neighboring Fourier coefficients will be much greater

4J First harmonic at F_{1000} and $F_{999,000}$.
nth harmonic at F_{1000n} and $F_{1,000,000-1000n}$
Fourier coefficient amplitude falls as 1/n

5A For the FIR approach, complex digital filter is:

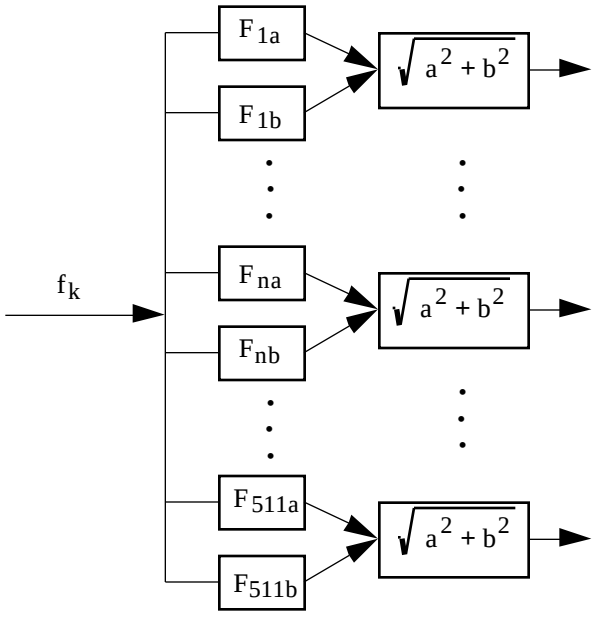
$$F_n = \sum_{k=0}^{511} f_k \left[\cos(2\pi nk/512) - i\sin(2\pi nk/512)\right]$$

For the IIR approach, the complex digital filter is:

$$F_n(t+\Delta t) = \left[F_n(t) - f_0 + f_{512}\right] \exp(i2\pi n/512)$$

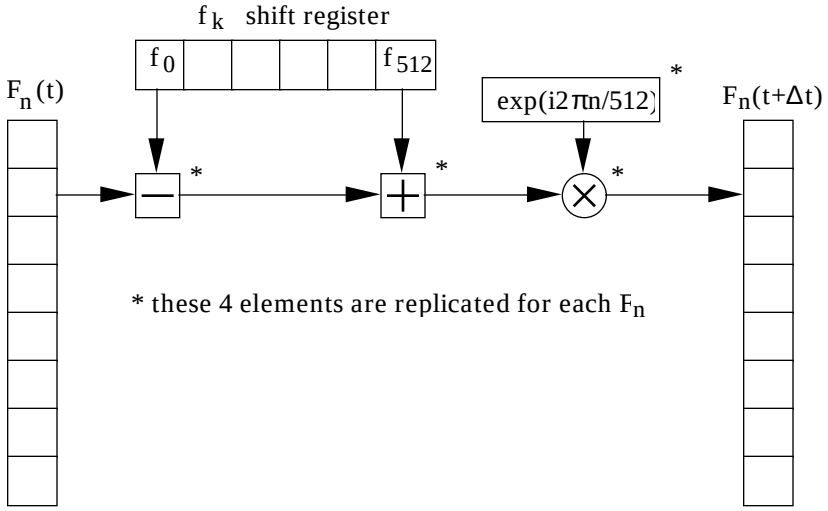
where $F_n(t)$ is the FFT of f_k, k = 0 to 511 and $F_n(t+\Delta t)$ is the FFT of f_k, k = 1 to 512 (one time step later).

5B For the FIR approach, the hardware schematic is:



where F_{na} is the real part and F_{nb} is the imaginary part of the complex Fourier coefficient F_n. Each processor requires access to all f_k.

For the IIR approach, the complex $F_n(t+\Delta t)$ are derived from the $F_n(t)$ and the data f_k as follows



5C For FIR approach need 512 for real part, 512 for imaginary part, and 512 to take square root of sum of squares (modulus) – 1536 in all. Each of the first two processors must make 512 multiplications and additions.

For IIR approach need 512 to (i) add real part of new term, (ii) subtract real part of last term, (iii) phase shift, and 512 for similar operations for imaginary coefficients, and and 512 to take square root of sum of squares (modulus) – 1536 in all. Each processor only needs to make a few multiplications and additions.

145M Numerical Grades:

	7/8 x Lab	Midterm	Final	Total
Averages	662	95	162	918 (B+)
rms	42	7	24	63

145M Letter Grade Distribution

Letter Grade	Course Totals (1000 max)
A+	990
A	959, 967
A–	933, 945, 947, 947
B+	912, 913, 924
B	none
B–	none
C	789, 797