Solutions for Midterm #1 - EECS 145M Spring 2010

1.1 Edge-triggered D-type flip-flop:
one digital data input
one digital clock input
one digital data output
on every rising edge of the clock the output is set equal to the input
otherwise the output is held constant

1.2 Transparent latch:
one digital data input
one digital gate input
one digital data output
when the gate signal is high the output is equal to the input
when the gate signal is low the output is held constant

1.3 Tri-state buffer
one digital data input
one digital "output enable" input
one digital data output
when the "output enable" signal is high the output is equal to the input
when the "output enable" signal is low the output neither drives nor loads anything it is connected to (high impedance state)

1.4 Set-reset latch
one digital "set" input
one digital "reset" input
one digital output that is "set" and "reset" by the two inputs

2.1

Elements needed for full credit

- 8 separate lines from output port to trigger inputs of the 8 digital devices
- eight separate set-reset latches with each "set" connected to the "data available (pulse)" from the corresponding digital device

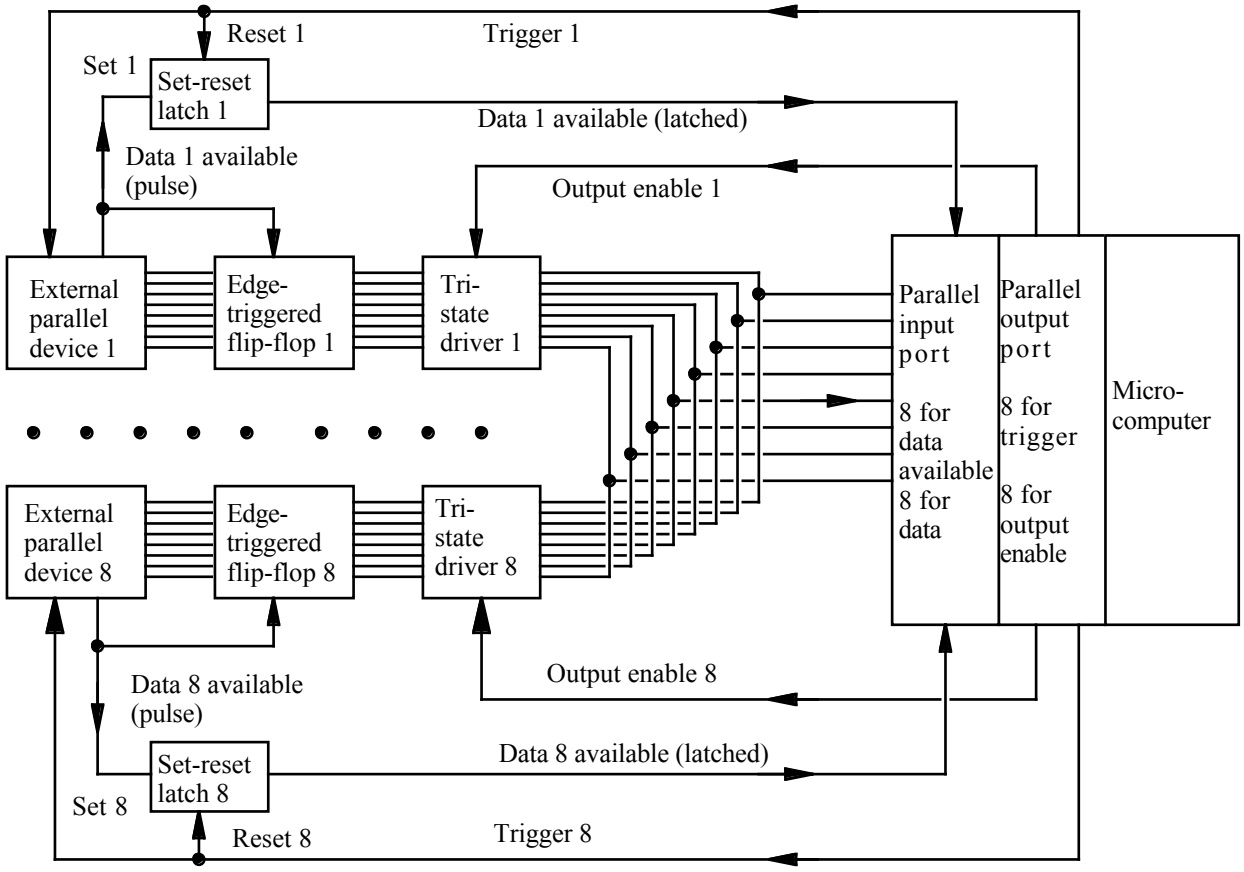
  no points off for eight one-shots set for an output pulse width several times 1 μs. This would work, but only if the computer reads the input port in a tight loop. It would not work if the computer were multi tasking and was not able to read the input port frequently enough.

  [5 points off if no set-reset latches to convert the very brief data available pulse into a persistent signal that the computer can read and reset]

- eight 8-bit transparent latches or edge-triggered flip-flops with control inputs connected to the "data available (pulse)" from the corresponding digital device

  [5 points off if no data buffer to convert the very brief data pulses into persistent signals that the computer can read]
- 8 data lines from each digital device connected to the inputs of the corresponding latch or flip-flop
- eight 8-bit tri-state drivers with inputs connected to the output of the corresponding latch or flip-flop

  [5 points off if no tri-state drivers, which are necessary to connect 8 x 8 data lines to 8 lines of an input port]
- The 8 output data lines of the eight tri-state drivers combined into an 8-line bus and connected to the digital input port
- 8 lines from the output port connected to the enable line of each tri-state driver
- 8 lines from the output port connected to the "reset" lines of the set-reset latches



2.2

- Output levels that set all 8 tri-state drivers to their high impedance mode
- Output a high-low-high to the trigger input of digital device #1 (this resets set-reset latch #1)
- Read the input line connected to set-reset latch #1 in a tight loop and exit when it becomes "set"

- Output the level that enables only tri-state driver #1
- Read and store the 8 data lines
- Output levels that set all 8 tri-state drivers to their high impedance mode
- Output a high-low-high to the trigger input of digital device #8 (this resets set-reset latch #8)
- Read the input line connected to set-reset latch #8 in a tight loop and exit when it becomes "set"
- Output the level that enables tri-state driver #8
- Read and store the 8 data lines
- Output levels that set all 8 tri-state drivers to their high impedance mode

3

- Acquire a computer with a digital I/O port and an internal clock
- Connect a pushbutton switch to one line of the digital input port and one line of the output port to an amplifier and fast indicator light (like an LED)
- Write a computer program that detects a pushbutton, waits a random delay, prompts the subject by turning on the light and measures the time until the pushbutton is pressed
- Select a large number of candidates representing group d (racecar drivers) and group p (jet fighter pilots)
- After initial training and a good nights sleep, take as much reaction time data as possible, allowing for rest periods
- Compute the average reaction times $\overline{d}$ and $\overline{p}$, the standard deviation of the samples σ_d and σ_p, and the standard errors of the mean $\sigma_{\overline{d}}$ and $\sigma_{\overline{p}}$ and compute Student's t:

$$t = \frac{\Delta}{\sigma_\Delta} = \frac{\overline{d} - \overline{p}}{\sqrt{\sigma_{\overline{d}}^2 + \sigma_{\overline{p}}^2}} = \frac{\overline{d} - \overline{p}}{\sqrt{\sigma_d^2 / m_d + \sigma_p^2 / m_p}}$$

- Look up the probability of exceeding this value of |t| by chance. If the probability is < 0.1%, then the group with the lowest average has a faster reaction time.

[2 points off for only a few subjects or number not given (the task was to compare the groups, not individuals)]

[2 points off if number of trials not given- this should be large (you can't determine the reaction time of a test subject very well with just a few measurements)]

[5 points if program steps not described in sufficient detail]

[3 points off if no delay between loop start and prompt]

[5 points off if hardware not described in sufficient detail]

[3 point off if Student's t calculation not mentioned]

[2 points off if statistical significance not related to the P(>|t|) value]

EECS145M Midterm #1 class statistics:

Problem	max	average	rms
1	24	21.7	2.9
2	40	30.2	6.1
3	36	32.4	1.9
total	100	84.3	7.5

Grade distribution:

Range	number	*approximate* letter grade
60-64	0	F
65-69	0	D
70-74	2	C
75-79	4	B
80-84	3	B
85-89	3	A
90-94	3	A
95-99	2	A+
100	0	A+