

Solutions for Midterm #1 - EECS 145M Spring 2004

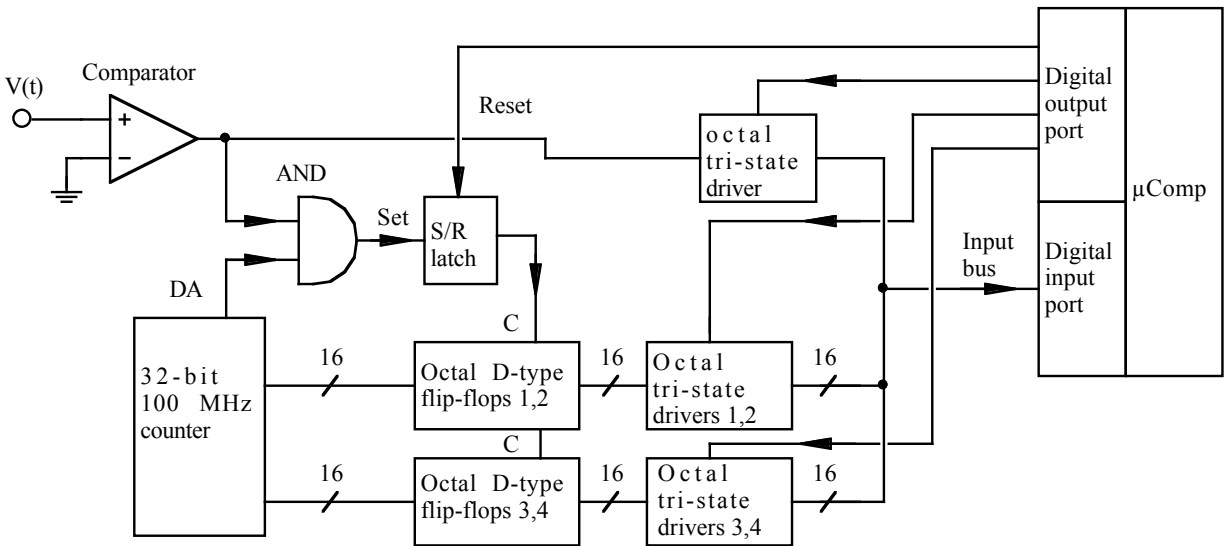
- 1a** The edge-triggered D-type flip-flop has a digital input D, a clock input C, and a digital output Q. On a rising edge of C, Q is set equal to D. Otherwise, Q is held constant.
- 1b** The sample-and-hold amplifier has an analog input, a control input, and an analog output. The control line selects sample mode (output = input) or hold mode (output held constant)
- 2** This problem had two challenges (1) how to latch data changing every 10 ns and (2) how to read 32 bits of those data using a 16-bit input port. Latching the data required using the DA pulse (to know when the data were stable) and the comparator (so that the data were latched only once per cycle of $f(t)$). Reading 32 bits of data with a 16 bit input port required tristate buffers that were controlled by the computer. Latching had to be done in hardware in nanoseconds, but reading was limited by the speed of the computer (microseconds). Relevant Design Tip slides were # 6, 10, 11, 16, and 23.

Essential features for a successful solution:

- Comparator detects zero crossing
- DA from counter AND comparator used to latch data on flip-flops
- Counter data latched only once per comparator cycle (computer reads comparator and resets S/R latch)
- Tri-state buffers used to read 32 bits from flip-flops into 16 bit input port
- Tri-state buffers enabled by computer output port

[4 points off for a design that merely counts comparator cycles in one second- this is not nearly as accurate as timing the interval between comparator pulse edges with a 100 MHz clock]

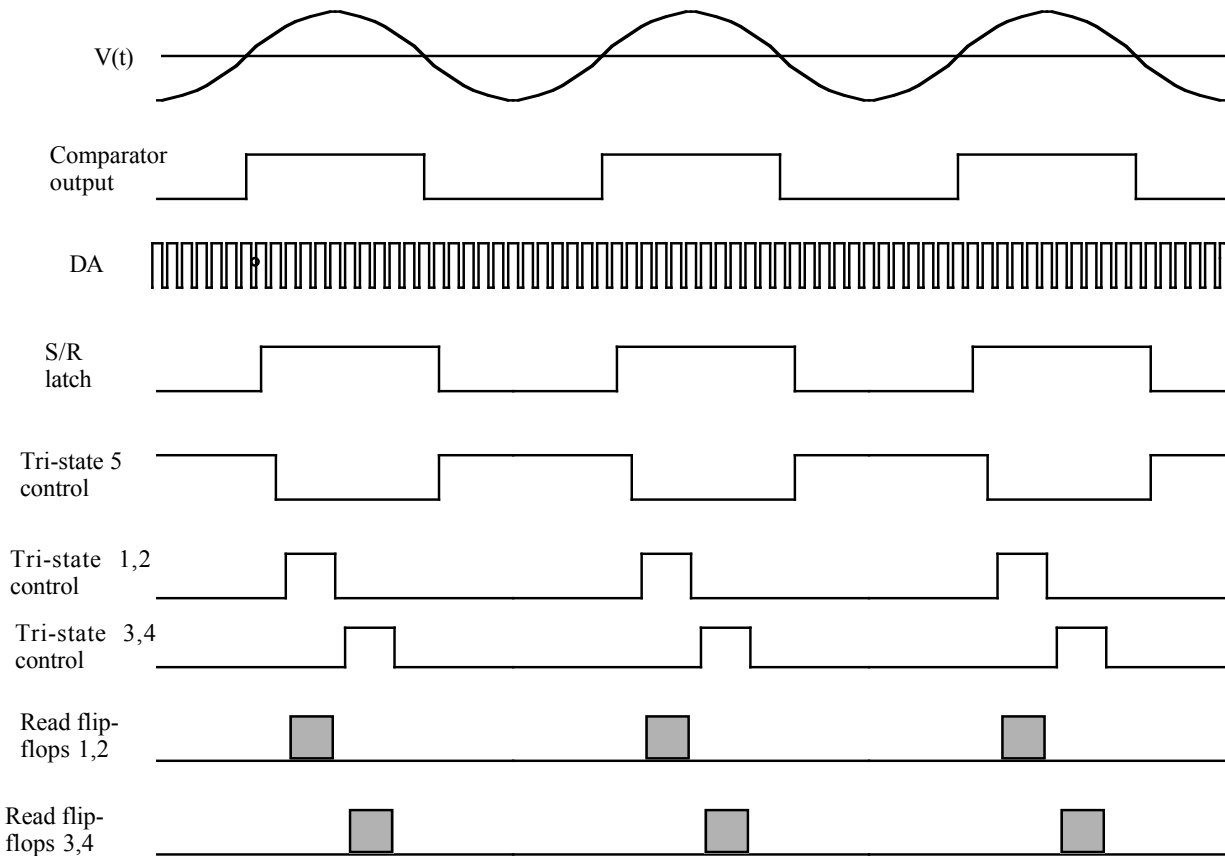
2a



- 2b**
- 1 the program sets $i = 1$
 - 2 program resets the S/R latch
 - 3 program enables tri-state 5 to connect only the S/R latch to input bus*

- 4 on next positive zero crossing of $V(t)$, comparator out goes high and S/R latch is set by the next rising edge of the DA pulse (within 10 ns)
 - 5 S/R latch strobes all 32 bits of the counter onto the four octal D-type flip-flops (since DA is high, the data are stable)
 - 6 meanwhile, the program has been reading the comparator output and detects the zero crossing of $f(t)$ (may take 1-2 microseconds)*
 - 7 the program enables tri-state 1 and 2 to connect only bits 1-16 stored on D-type flip flops 1 and 2 to the input port*
 - 8 the program reads counter bits 1-16*
 - 9 the program enables tri-state 3 and 4 to connect only bits 17-32 stored on D-type flip flops 3 and 4 to the input port*
 - 10 the program reads counter bits 17-32*
 - 11 the program packs the data into a 32 bit word and stores it at $T(i)$
 - 12 the program increments index i
 - 13 the program loops back to step 2 for one second (this need not be exact)
 - 14 the program sets $N = i - 1$
 - 15 the program computes the frequency as $[100 \text{ MHz}][N-1]/[T(N)-T(1)]$ and displays the result. [If $T(N)$ is less than $T(1)$ the counter has cycled through zero (happens every 40 s) so add 2^{32} to $T(N)$]
- * 1 microsecond read or write (6 total)

2c



- 2d** Since the measurement time was specified to be one second, the lowest frequency that can be measured is 1 Hz.

Since the program does three writes (to the tri-state drivers) and three reads (one to detect the S/R latch and the other two to read the counter data), the minimum cycle time is 6 microseconds, which corresponds to a maximum frequency of 167 kHz. Since the other operations take a bit of time also, a realistic maximum frequency would be 150 kHz.

[2 points off for 0 Hz minimum] [2 points for 100 MHz maximum]

- 2e** At the minimum frequency of 1 Hz, $N=2$, $T(2) - T(1)$ will be $10^8 \pm 1$, and the accuracy will be 10^{-8} Hz.

Note: $\Delta f = [1 \text{ Hz}] [10^8/10^8 - 10^8/(10^8+1)] = [1 \text{ Hz}] [1 - 1/(1+\epsilon)] \approx [1 \text{ Hz}] [\epsilon]$, where $\epsilon = 10^{-8}$

At the maximum frequency of 150 kHz, $N \approx 150,000$, $T(2)-T(1)$ will be $10^8 \pm 1$, and the accuracy will be $(150,000)(10^{-8} \text{ Hz}) = 0.0015 \text{ Hz}$.

[Note: $\Delta f = 150,000 [10^8/10^8 - 10^8/(10^8+1)] \approx [150,000 \text{ kHz}] [\epsilon]$, where $\epsilon = 10^{-8}$]

- 3** The solution to this problem was the digital deglitcher given in Design Tip slides #11 and 12 [4 points off for rejecting outlying values, or using a different counter, or using a transparent latch without describing how a DA pulse could be generated]

[2 points off for generating a DA pulse but using it to control a sample and hold amplifier, which is an analog device with limited bandwidth and settling time (see slide 152)]

- 4** For problem 4, 1 point was deducted for each wrong answer and 1 point was deducted for each missing correct answer]

- 4a** TR, FL

[SA, DS, HF convert only after they have been given a start conversion pulse- see Design Tips slide 22]

- 4b** SA, DS, HF

[see Design Tips slide 22]

- 4c** FL

[TR and DS would require 65,000 steps to sweep the full range- not possible in 10 ns]

[SA would require 16 steps- also not possible in 10 ns]

[HF would require D/A conversion, difference amplifier settling, second D/A conversion – all in 10 ns- not currently feasible]

- 4d** SA, HF

[DS and TR would require $20 \text{ kHz} \times 2^{16} = 1.3 \text{ GHz}$ clock speed]

[FL would require 65,000 comparators- not currently feasible]

- 4e** DS

[TR, SA, and HF have internal D/A converters that contain resistors whose accuracy is important]

[FL has a resistor string that sets the reference voltages for the comparators]

- 4f** SA, HF

[DS takes a time average and does not need a steady input]

[TR and FL track the input in real time]

EECS145M Midterm #1 class statistics:

Problem	max	average	rms
1	16	15.3	1.1
2	46	22.9	10.1
3	8	4.8	1.7
4	30	21.9	4.1
total	100	64.9	13.4

Grade distribution:

Range	number	<i>approximate</i> letter grade
40-44	0	
45-49	4	C
50-54	1	C+
55-59	1	B-
60-64	2	B
65-69	4	B+
70-74	2	A-
75-79	2	A
80-84	0	
85-89	2	A+
90-94	0	
95-99	0	
100	0	